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Field-store standards conversion:

description of the CO6/506 converter

No. 1970/37

Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION

RESEARCH DEPARTMENT

FIELD-STORE STANDARDS CONVERSION: DESCRIPTION OF THE C06/506 CONVERTER

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FIELD-STORE STANDARDS CONVERSION: DESCRIPTION OF THE C06/506 CONVERTER

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FIELD-STORE STANDARDS CONVERSION: DESCRIPTION OF THE C06/506 CONVERTER

Summary

The report gives a technical description of the BBC Mk. 2A (C06/506) field-store standards converter, which operates in the direction 525/60 NTSC to 625/50 PAL. The equipment is very complicated and a preliminary simplified description is given to help with the later sections; throughout the report, the description is limited to the block diagram level and much detail has been omitted. The report ends with a section describing selected aspects of special interest.

1. Introduction

1.1. General

The basic concept of the Advanced* Field-Store Standards Converter has already been described in a previous report[1] and a number of other reports[2,3] and papers[4,5] have been published describing some aspects of the converter in more detail. In this report, a technical description is given of a Field-Store Standards Converter designed to convert in the direction 525/60 NTSC to 625/50 PAL. This was the form of converter which was introduced into service for the first time on the occasion of the 1968 Mexico City Olympic Games and which has been in continuous service ever since.

The report does not attempt to give a description of each unit; considerable complexity is involved and all descriptions are restricted to the block diagram level of detail.

1.2. Main features of the converter

Input signals on the American 525/60 NTSC television scanning standard are converted to the European standard of 625/50 PAL (or 625/50 SECAM if suitable output transcoding equipment is used).

The converter also accepts signals on the American 525/60 monochrome** standard for conversion to the 625/50 monochrome standard used in Europe and elsewhere.

A non-integral ratio of field frequencies is permitted between the input and output scanning standards. This is necessary because the field frequency of 525/60 NTSC colour television signals is 59·94 Hz, compared to the value of 50·00 Hz used in Europe; furthermore, the tolerance on American colour television scanning frequencies is some ten or eleven times less tight than in Europe. A converter with a fixed ratio (e.g. 6:5) between its input and output field frequencies could not produce a standard output signal from a standard input signal.

The output signal is synchronous with the locally generated pulses etc. and can be cut, mixed and faded with other colour signals exactly as if the converter were a local television source.

Following upon any interruption of the input signal or a 'cut' from one television signal source to an unrelated source, the output signal from the converter becomes re-established and is fully synchronous within one tenth of a second. The output synchronising pulses are continuous and remain unchanged whenever the input signal suffers an interruption or other disturbance; this is a particularly useful feature when converting signals received from communication satellites. The continuity of the output synchronising pulses affords complete protection for a video tape recorder which may be recording the converted signals and which would otherwise take many seconds to resynchronise following an interruption.

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* The term 'Advanced' is used to distinguish this converter from an earlier field-store standards converter developed by BBC Designs Department and known as the 'Simple' converter; only the advanced converter is described in this report and the term 'Advanced' is henceforth not used.

** The American monochrome field scanning frequency is nominally 60 Hz whereas the field scanning frequency for colour is 59·94 Hz.

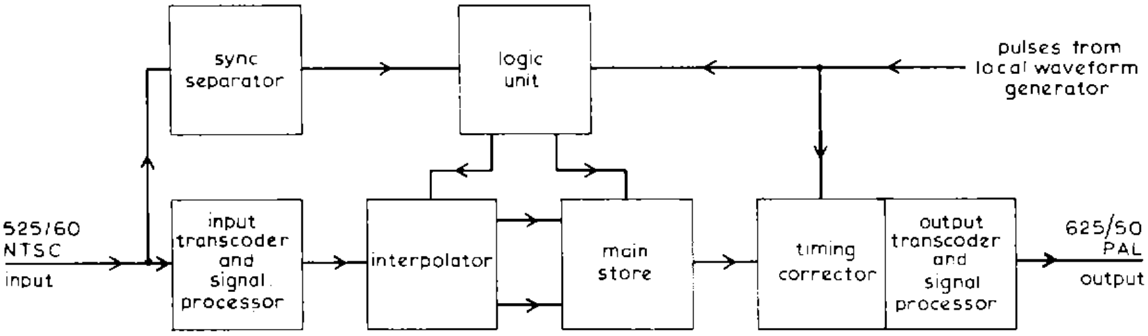
sync separator
logic unit
pulses from local waveform generator
525/60 NTSC input
input transcoder and signal processor
interpolator
main store
timing corrector
output transcoder and signal processor
625/50 PAL output

Fig. 1.1. – Simplified block diagram of converter

1.3. Simplified description of operation

The simplified operation will be described with reference to Fig. 1.1. The same principle of operation can be applied to conversion in the opposite direction, i.e. from 625/50 to 525/60.

This simplified description is intended to give an outline of the operation of the converter which will help in the later sections.

1.3.1. Input transcoder and input signal processing

The input 525/60 NTSC signal enters the transcoder where its colour coding is changed to a special form suitable for the passage of the signal through the standards converter. This 'intermediate' system of coding is similar to NTSC, except that a higher frequency of colour subcarrier is used so as to place the chrominance signals outside the frequency-band occupied by the luminance signals. The frequency of the intermediate subcarrier is also chosen to be a multiple of the line frequency in order to simplify the action of the interpolator which follows.

1.3.2. Interpolator

The transcoded signal is received by the Interpolator where all the necessary television line signals* are produced for the output picture signal; this involves the generation of signals for 100 extra lines per picture. The interpolated signals are formed by combining selected signals from adjacent television lines and fields; the method of selection is chosen both to minimise geometric distortion of the picture and to preserve the satisfactory portrayal of movement in the televised scene.

Two connections are needed to handle the interpolator output because each input television picture signal is already provided with its full complement of line signals and the generation of signals for the extra lines means that periodically two differently interpolated signals must occur at the same time.

1.3.3. Main store and logic unit

The main store is a kind of marshalling yard which, by introducing a systematically increasing signal delay, re-times the signals from the interpolator so as to make room for the extra television lines. The output from the main store consists of a stream of television line signals, all in the correct order.

The main store is formed from a switched network of ultrasonic quartz delays and is controlled by the logic unit, which determines the delay to which each television line is subjected according to the results of measurements which it makes of the relative timings of the input and output television signals.

At regular intervals (usually every sixth input field), the delay in the main store is re-set, thereby dropping or omitting the field contained in the store at that time. This would result in intolerable 'judder' on the output picture when an object moved within the scene, were it not for the fact that the output signals from the interpolator are arranged to include sufficient information from the omitted field to smooth out the judder.

1.3.4. Timing corrector and output signal processing

Although the output from the main store comprises television line signals in the correct order and with the correct average frequency, their timings are somewhat ragged and the function of the timing corrector is to ensure that they occur at the precisely equal intervals of time dictated by the local 625/50 television standard.

The signal at this stage is now in the 625/50 form, but the colour coding has to be changed from the intermediate system used in the converter to the PAL system required for broadcasting in Europe. Of course, the system of colour coding may be changed to any other form (e.g. SECAM) if desired.

1.3.5. Physical layout

The converter is housed in seven bays, and is shown in Fig. 1.2.

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* In this report the term 'line signal' is sometimes used to describe a signal carrying the picture information for one television scanning line.

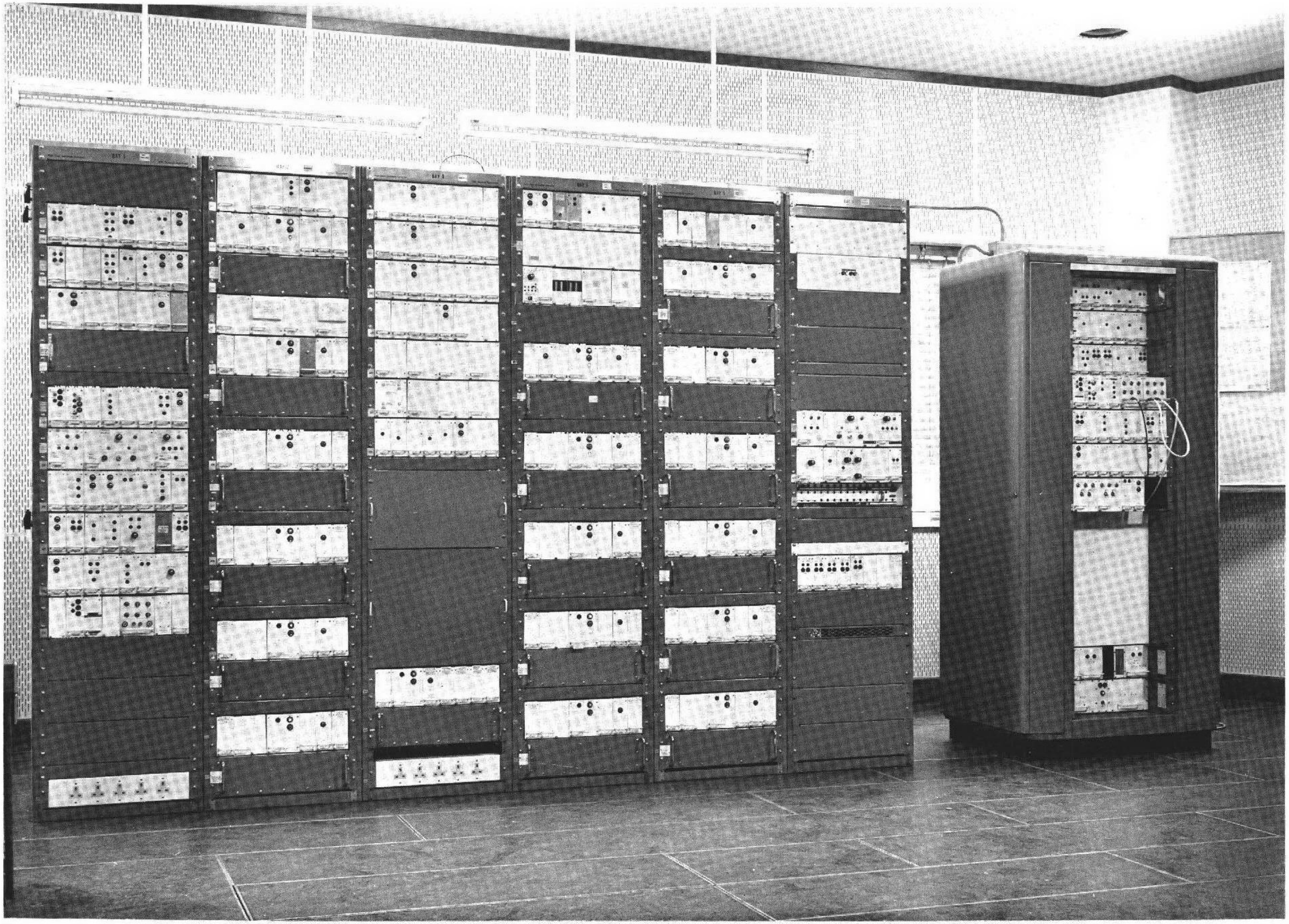


Fig. 1.2. – Field-store standards converter C06/506 installed at Television Centre

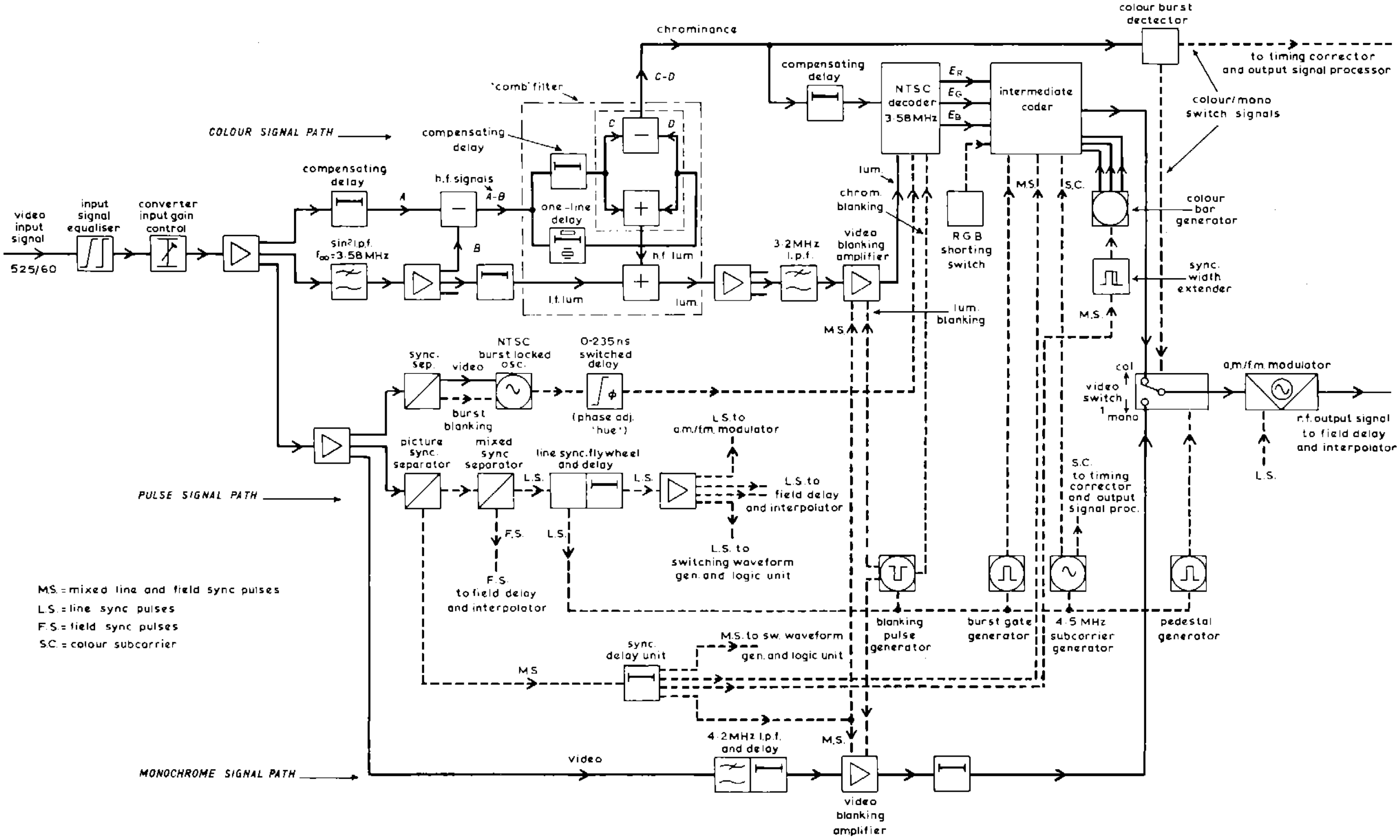


Fig. 2.1. – Input signal transcoder and processor

2. Input transcoder and signal processor

2.1. General

There are three main signal paths in the input signal processor as may be seen in Fig. 2.1. These paths are:

(a) The colour signal path
(b) The monochrome signal path
(c) The pulse path (common for both monochrome and colour video signals).

The colour or monochrome path is selected automatically by a switch within the input signal processing unit. The colour path is selected whenever the input signal carries a colour burst and the monochrome path is selected in other cases.

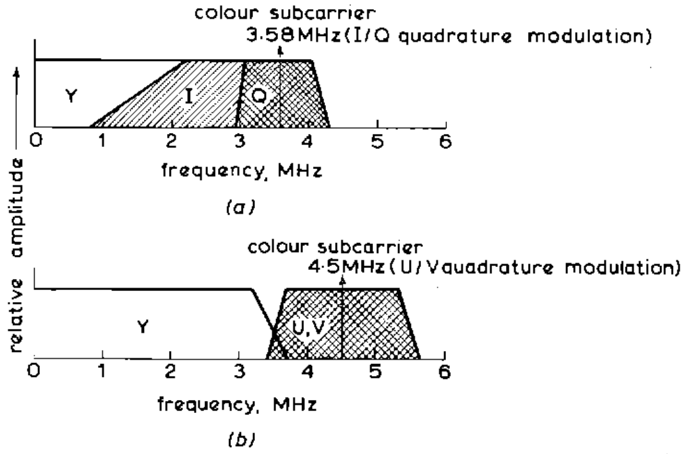
Modulation of the picture and synchronising signals on to an r.f. carrier takes place in the final stage; this carrier is suitable for transmission through the quartz delays in the interpolator and main store of the converter. The input signal processing is described below.

2.2. Colour input signal processing

2.2.1. Principle

The frequency of the colour subcarrier in the NTSC input signal is such that, in a plain coloured area, the phase of the chrominance signal at any given point along one television line of a field differs by 180° from that at the corresponding point on the next line of the same field. If this signal were used for transmission through the converter it would then not be possible to average between successive lines for interpolation purposes. To avoid this difficulty[6] the input signal is transcoded to an alternative form of NTSC signal known as the 'intermediate' signal in which the subcarrier frequency is an integral multiple of the input line frequency. Moreover, since it is necessary to separate the luminance and chrominance components of the intermediate signal after standards conversion, the subcarrier frequency is increased to place the chrominance signal outside the limited luminance band, permitting adequate separation by simple filters. Fig. 2.2. shows the main features.

The actual intermediate colour subcarrier frequency is 4·5 MHz, corresponding to 286 times the input line frequency. It is also an integral multiple (288) of the output line frequency. As a result, the possible interference patterns which might arise from beats with either the input (3·58 MHz), or output (4·43 MHz) colour subcarriers have a half-line or a quarter-line offset relationship, respectively, and the visibility of such interference is accordingly minimised.



(a)

(b)

Fig. 2.2. – Spectra for input and intermediate colour signals

2.2.2. Practical method

The basic function of the colour path is to transcode and translate the input signal using established techniques.[7] A delay-type or 'comb' filter[7] employing a one-line delay is used to separate the luminance and chrominance components of the input signal in order to minimise the possible spurious effects[7] from imperfect separation.* A conventional NTSC decoder (demodulating along the I and Q axes of the chrominance signal) then recovers the E_R, E_G and E_B (R G B) components of the input signal (decoding completely to RGB components is not essential for transcoding purposes but has the advantage that alignment and testing of the decoder and coder can be carried out in the normal manner using standard RGB signals). The effective luminance bandwidth of the decoded NTSC video signal is about 3·2 MHz.

The decoded signals, stripped of all input synchronising information, are fed to the intermediate coder. This consists of a standard PAL coder with minor modifications to remove the V-axis switching and to effect the small subcarrier frequency change from 4·43 MHz to 4·5 MHz. The chrominance component of the intermediate signal is thus formed and transmitted through the converter using double-sideband, quadrature amplitude-modulation by colour difference signals, with an effective chrominance bandwidth of

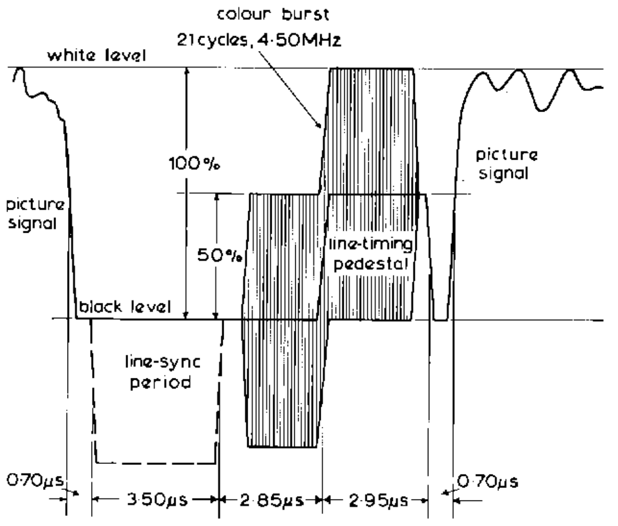


Fig. 2.3. – Intermediate signal video waveform: line blanking period

about ±1 MHz. The colour-burst used for the intermediate signal is non-standard in that its peak-to-peak amplitude is 0·7 V and it has a duration of 21 cycles. The purpose of the large-amplitude and long duration of the burst is to achieve as high a signal-to-noise ratio as possible in the chrominance control circuits at the output of the converter. Fig. 2.3 shows the waveform of the signal after input processing. It will be seen that the mean level of the second part of the colour-burst is raised on a 'pedestal'. This pedestal is included for timing purposes, as will be seen later, but has the additional advantage of minimising the subjective effects of differential gain and phase distortion.

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* The action of the comb filter also causes the chrominance and higher-frequency luminance components to have a mean delay of half a line period and they are consequently vertically misregistered with the lower-frequency luminance components. However, the chrominance signal will suffer a further, similar, half-line delay when the converted PAL output signal is decoded and this would make the total vertical chrominance/luminance misregistration equal to one line. These two effects are pre-corrected in the converter by delaying the luminance signal to the output PAL coder by a corresponding one-line period.

2.3. Monochrome input signal processing

As shown in Fig. 2.1, a monochrome input signal undergoes bandwidth restriction (to the 4·2 MHz specified for the monochrome 525/60 standard) followed by black-level clipping, line and field blanking and delay to obtain the correct output signal timing.

Selection of the monochrome or intermediate coded signals is by means of the video switch controlled either automatically by a colour-burst detector, or by a manual over-ride switch.

2.4. Synchronising pulse processing

Mixed synchronising pulses (syncs), extracted from the input signal using a conventional sync separator, are delayed appropriately and fed to various units in the input signal processor for blanking purposes. They are also fed to the logic unit controlling the interpolator and main store of the converter.

Separate line and field syncs are derived from the recovered mixed syncs; field syncs are fed to a logic unit controlling the field delay in the interpolator and line syncs are fed to the flywheel line sync regenerator unit. This provides pulse signal outputs of appropriate timing for various functions in the input signal processor, the field delay and interpolator, and the main store. The processes of line/field separation, flywheel line sync regeneration and waveform delay use established techniques which do not need elaboration in this report.

The purpose of the flywheel is to provide accurately-timed, jitter-free, line sync pulses from an input signal which may be noisy or which may have line sync pulses jittering in relation to stable picture information. (The latter condition may seem surprising but nevertheless has been observed on signals received via the satellite link from America.) Accurate line timing information is essential for two main purposes. First, for the Field delay, which is servo-controlled to an accuracy of about 9 ns and which operates by comparing delayed and undelayed line syncs (see Section 3). Second (and even more important) for the timing correction of the converted output signal (see Section 6); in this connection it is relevant to describe the purpose of the pedestal inserter shown following the video switch in Fig. 2.1. As will be discussed in Section 2.5, the r.f. carrier which conveys the signal through the quartz delays of the converter is frequency modulated (f.m.) by the picture signals and amplitude modulated (a.m.) by the line sync signals. A disadvantage of this dual modulation system, however, is that any distortion suffered by the f.m. signal may differ from that suffered by the a.m. signal. As a result, the timing of the demodulated a.m. line syncs may not be related with sufficient accuracy to the timing of the accompanying picture signals. To overcome this difficulty, a pedestal is inserted during the back porch period which, because it is transmitted via the f.m. system, is suitable for line-timing purposes; the less accurate a.m. line syncs are used only to gate out the pedestal. To accommodate the pedestal and the lengthened colour-burst, a slightly short line sync pulse is used for transmission through the converter.

2.5. A.M./F.M. modulation

The ultrasonic quartz delays in the interpolator and main store of the converter operate over a frequency band of about 25 to 35 MHz. It is therefore necessary to modulate the intermediate signal on to an r.f. carrier for transmission through the delays. In deciding upon the type of modulation to be used, the available bandwidth and the switching in and out of delays, with their inevitable gain and performance variations, were the main considerations. As a result of studies,[2,3,8] an asymmetric sideband, low-deviation frequency-modulation system[9] was chosen for the picture signals (including of course the line-timing pedestal described in Section 2.4.). The carrier frequency corresponding approximately to mid-grey is 32 MHz, with a deviation of ±0·5 MHz, the sense being such that the frequency is reduced for white and increased for black. The deviation characteristic is somewhat non-linear but is matched by a complementary characteristic in the demodulator (see Section 6). Negative modulation was chosen to reduce the visibility of spurious echoes caused by delay lines. The most troublesome of these were associated with the line-blanking period; by using negative modulation, black level is arranged to be on the vestige side of the vestigial-sideband (v.s.b.) filter characteristic and hence lower in level. Radio frequency pre- and de-emphasis, and v.s.b. filtering, are described in Sections 3 and 6.

The video line sync pulses are impressed on the carrier in the form of amplitude-modulation, the carrier being reduced to zero during the line sync period. The primary object of this is to provide an interval of zero carrier during which switching takes place in the interpolator and main store. If switching were to occur with a carrier present, large-amplitude transients might be generated (due to the unrelated phases of different f.m. carriers) with consequent undesirable overloading effects.

An advantage accrues from the use of a.m. for the line syncs in that the available deviation range for the video information is increased by about 40% with a corresponding improvement in signal-to-noise ratio performance.

3. Interpolator

3.1. General considerations

Conversion between two television standards involving

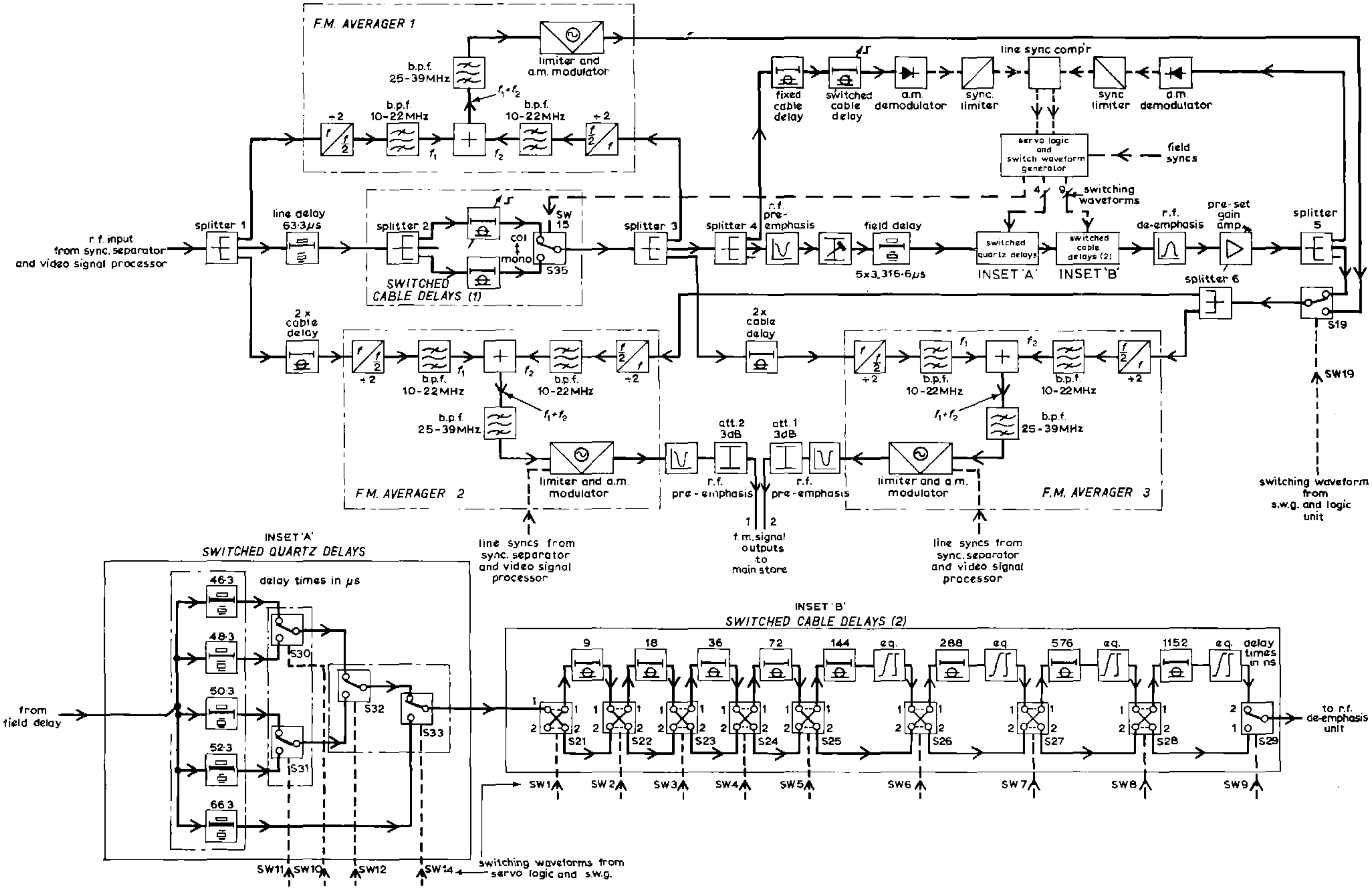


Fig. 3.1. – Field delay and interpolator

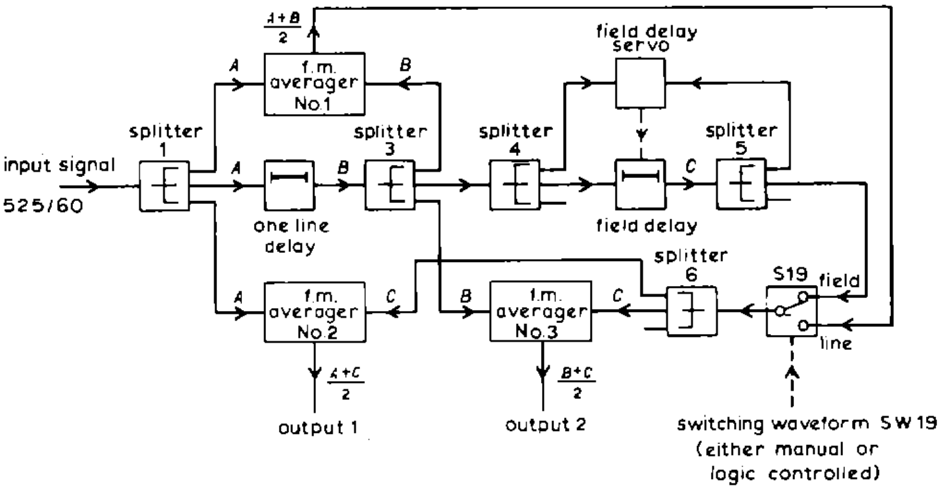


Fig. 3.2. – Interpolator simplified schematic

a change in both the number of lines and the number of fields per second can result in two important forms of picture distortion. These are well-known, and a full description can be found elsewhere,[1,11,12] but they may be briefly summarised as follows:

(a) Geometric distortion caused by the disturbance of the relationship between picture information and line structure. This often can be seen in the form of serrations on sloping edges and, due to the effects of interlace, spurious movement within the picture is also created.

(b) Impairment of movement portrayal; objects in the scene which should be moving smoothly appear to jump through a distance corresponding to two field intervals whenever an input field is omitted. This gives rise to a serious subjective effect known as movement 'judder' or 'cogging' at the frequency of field omission.

The interpolator, which precedes the main store has been designed to provide compensation for both the effects listed above.

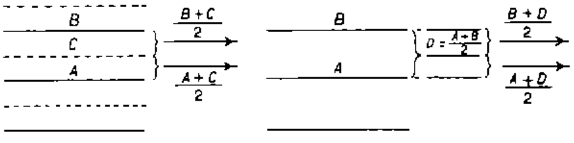
In the description which follows, reference is made to the block diagram Fig. 3.1. However, for ease of explanation, a simplified block diagram has been prepared (Fig. 3.2) showing the layout of the field delay and interpolator. The description also contains references to 'f.m. averagers'. These have been developed in order to perform signal-averaging between the frequency-modulated carriers themselves, thus avoiding the necessity of demodulation before interpolation can take place. The method of averaging is of special interest and is discussed more fully in Section 7.1; it is also the subject of a separate report.[6]

Three types of interpolation have been provided, these have been called 'Field' interpolation, 'Line' interpolation and 'Mixed' interpolation. 'Line' and 'Field' interpolation are intended to be used only under emergency conditions.

3.2. Field interpolation

'Field' interpolation involves the use of a field delay in order to provide picture information from two successive fields simultaneously. With reference to Fig. 3.2, consider the case where the switch S19 is in the position marked 'Field'; for this operation the output of f.m. Averager No. 1 is not used.

Fig. 3.3(*a*) represents a magnified part of the incoming raster with the lines from two successive fields represented by hard and dotted lines respectively. Consider one television line, say A, which, for a certain period, forms the output of Splitter No. 1. At the same time line B, (the previous line of that field), emerges from the one-line delay, and appears at Splitter No. 3; similarly, line C (from the previous field, and occupying the interlaced space between lines A and B), is available from the field delay via Splitter No. 5. In such conditions the output of Averager No. 2 is the average of A and C, and the output of Averager No. 3 is the average of B and C. These outputs represent new lines $(A + C)/2$ and $(B + C)/2$ respectively; they are the signals produced by the interpolator in the 'Field' condition.



(a) (b)

Fig. 3.3. – Interpolation between raster lines

From these two outputs a selection is made of whichever is the closest in picture content to the ideal for the appropriate new line in the 625-line structure. The selector switches for this operation are controlled by the main store logic, and are shown as S1 and S2 at the beginning of block diagram Fig. 4.1.

It should be noted that while the field delay contributes towards satisfactory interpolation between lines, it does not, in this method of interpolation, improve the movement portrayal. Indeed, because every output line from the interpolator consists at all times of equal proportions from two successive fields, whenever there is movement a double-image effect is seen. While this tends to have a blurring effect on moving edges, an effect which has been considered to enhance the illusion of speed, tests have shown that it does not greatly reduce the subjective effect of movement judder.

3.3. Line interpolation

'Line' interpolation is represented by Fig. 3.3(*b*) and Fig. 3.2 with S19 in the 'Line' position. This brings Averager No. 1 into use and disconnects the field delay. With reference to Fig. 3.3(*b*), consider the same two lines A and B. The interlace line C which was previously available at the output of the field delay has now to be synthesised as, say, line D. This is achieved by averaging A and B together in Averager No. 1, to form $(A + B)/2$ (which is line D). Thereafter, the interpolator functions as before to produce the interpolated signals $(B + D)/2$ and $(A + D)/2$. Thus, the output is derived from a single input field; this not only results in inferior vertical resolution, but is unable to provide compensation for movement judder.

3.4. Mixed interpolation

In this method of interpolation, S19 is switched systematically (during the field-blanking period) according to a pre-determined sequence derived in the main store logic unit. During each cycle of 6 input fields (5 output fields), the time spent on field and line interpolation is divided in the ratio 2 : 3 respectively.

Fig. 3.4 represents the error in the mean position of a moving object expressed as a function of output field number (i.e. time). The error also is expressed in units of field duration which, with a smoothly moving object, describes the relative error in its position. On line and field interpolation, the error is seen to cycle once every five output fields, the graphs of line and field interpolation representing images whose mean positions are displaced by half of one field period. This half period arises from the double image produced by the field interpolator, the eye tending to see the object midway between the two objects of the double image. The advantages of mixed interpolation now become obvious, since by switching between the two systems at the appropriate times, the overall amplitude of judder is roughly halved, and the frequency of judder is doubled. Both these effects on their own would be considered beneficial. The effect of mixed interpolation is to degrade the vertical resolution relative to that obtained

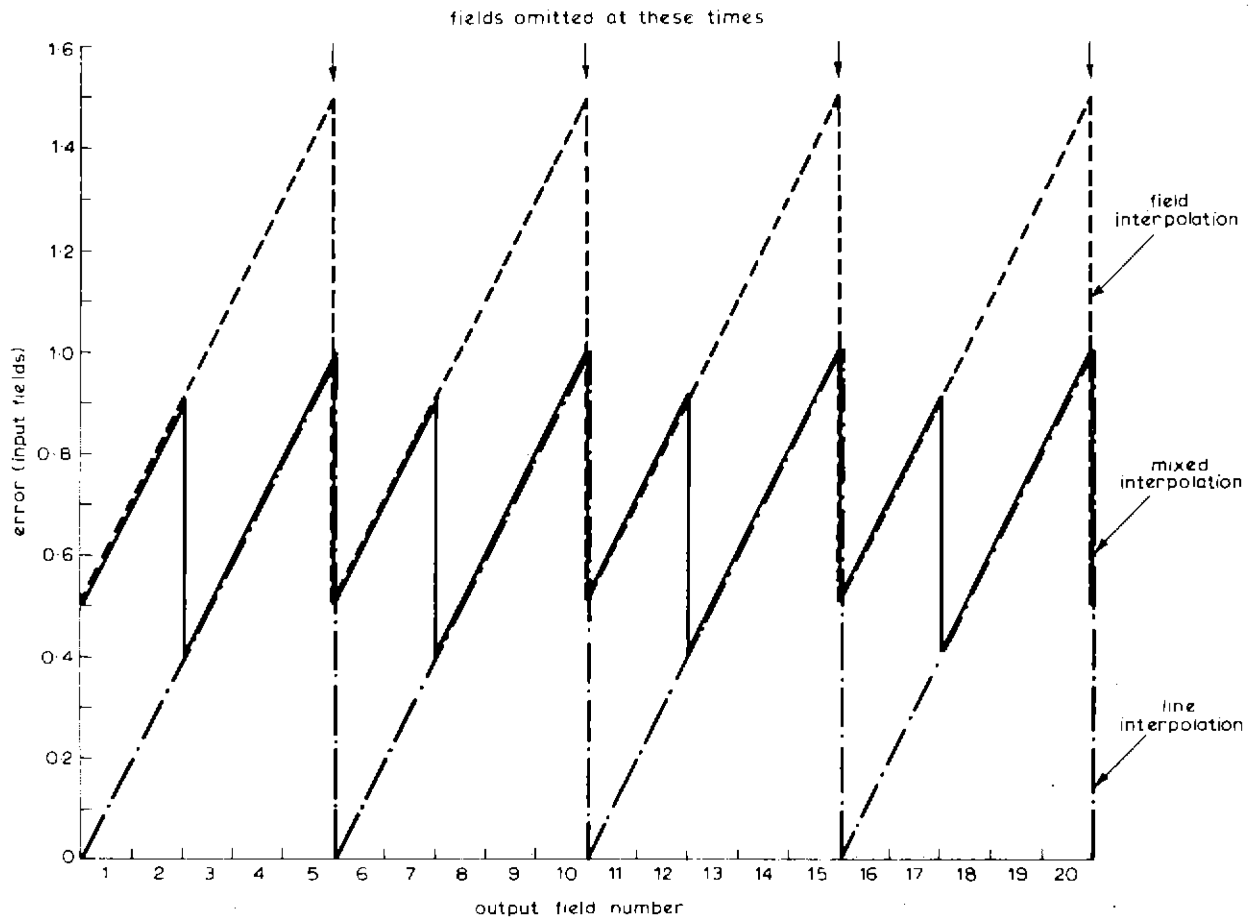


Fig. 3.4. — Movement interpolation: error in mean position of a moving object

from field interpolation alone, but this disadvantage must be weighed against the substantial improvement which is achieved in movement portrayal.

It is interesting therefore to note that with the interpolator in the 'Mixed' mode, the field delay has two separate functions. First, it provides better interpolation between lines than would otherwise be possible and second, it maintains adequate smoothness of object movement in the resultant picture.

3.5. Block diagram Fig. 3.1

(a) Field Delay and Servo[10]

All units between Splitters 4 and 5 are regarded as comprising the field delay. Pre- and de-emphasis units provide enhancement of high-frequency sidebands during the passage through the field delay. The field delay consists of five 3·316 ms ultrasonic quartz delays[8] with equalisers followed by five switched quartz delays of values 46·3, 48·3, 50·3, 52·3 and 66·3* μs. These are followed by switched cable delays with a total capacity of 2·395 μs.

A.M. syncs obtained from the signals before and after the field delay are compared in the line sync comparator. Two outputs from the comparator are used to trigger a binary counter contained in the servo logic unit. The counter stages are coupled to switched cable delays (with values arranged in ascending binary order from 9 ns to 1152 ns) such that the cable corresponding to a particular binary stage is connected in series with the field delay when that particular stage is activated. When mistiming of the line syncs across the field delay is sensed by the line sync comparator, pulses at line-sync rate appear at the appropriate logic-unit input and thus change the total delay value in 9 ns steps so as to compensate for the error. The delay then remains at this value until further correction is required. A second counter in the logic unit is used to determine which of the five switched quartz delays should be in circuit; a suitable command signal is produced during each field blanking interval whenever the switched cable delay value nears the end of its range. Four of the switched quartz delays provide sufficient range (in steps of 2 μs) to cover the wide delay variation required for monochrome operation; a fifth delay of 66·3 μs is used during colour operation only.*

An additional output from the servo logic operates two cable-delay trimmers for the one-line delay at the colour and monochrome centre frequencies.

(b) Fixed Cable Delays

There are three fixed cable delays each of length 200 ns. Their function is to compensate for the unavoidable inherent delay in F.M. Averager 1.

(c) F.M. Averagers

The method used to produce an average of two f.m. signals is discussed in Section 7.1. At this stage it is sufficient to say that the process involves limiting; because this changes the nature of the a.m. line-sync pulses, remodulation (of the carrier by pulses) takes place in the final unit of each F.M. Averager assembly. R.F. pre-emphasis is introduced before transmission of the interpolated carrier signal through the main store.

4. Main store

4.1. General

The main store, of which Fig. 4.1 is a block diagram, is formed mainly from ultrasonic quartz delays[8] and r.f. switches. It is here that interpolated line signals are selected, delayed and approximately synchronised with the 625/50 standard output pulses.

In the interpolator, two simultaneous sequences of line signals have been generated, describing interlaced fields at the input 525/60 standard and selection of the nearest line of the input picture to each 625/50 standard output television line by means of S1 and S2 (see Fig. 4.1) is carried out according to pre-determined waveforms. At this stage, one extra line has been generated for each five or six lines incoming and this extra line has to be accommodated by an increase in delay in the main store. The unit of delay is chosen to maintain the correct average output line frequency and, since fifty extra units are accumulated per field, the unit is one fiftieth of the difference between the field durations at the 525/60 and 625/50 standards. This can be shown to have the value of 66·333 μs, and has been designated the T unit.

4.2. Binary delay store

A progressive increase of delay up to 299 T units in steps of one unit is needed in the main store and is achieved by switching the signal among the quartz delays using the switches S3, S4 up to S15 as in Fig. 4.1.

The store used in the converter is a modified extension of the simple binary delay store shown in Fig. 4.2; processes in the nth stage of such a store are illustrated by Fig. 4.3. Rectangles numbered 1, 2, 3, etc. in 4.3(*b*) represent continuous sequences of signals at terminal points A_1 and B_1 of Fig. 4.3(*a*). After traversal of the delay or by-pass paths, the sequences of signals at A_2 and B_2 are shown in similar form by Fig. 4.3(*c*). If the switch is reversed according to the waveform of Fig. 4.3(*e*), the signals at A_3 and B_3 will be as represented in Fig. 4.3(*d*); by comparison of Figs. 4.3(*b*) and (*d*) it can be seen that the resultant signal sequences and the overlaps are both doubled in length.

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* American monochrome television operates with a nominal field frequency of 60 Hz; however, four switched quartz delays are needed to cover the wide tolerance. Colour signals operate on a tightly-controlled field frequency of 59·94 Hz (i.e. one part in 1000 lower than for monochrome). This means that the total field delay requires to be one part in 1000 (i.e. 16 μs) longer and, because of the narrow tolerance, one quartz delay (66·3 μs) is sufficient.

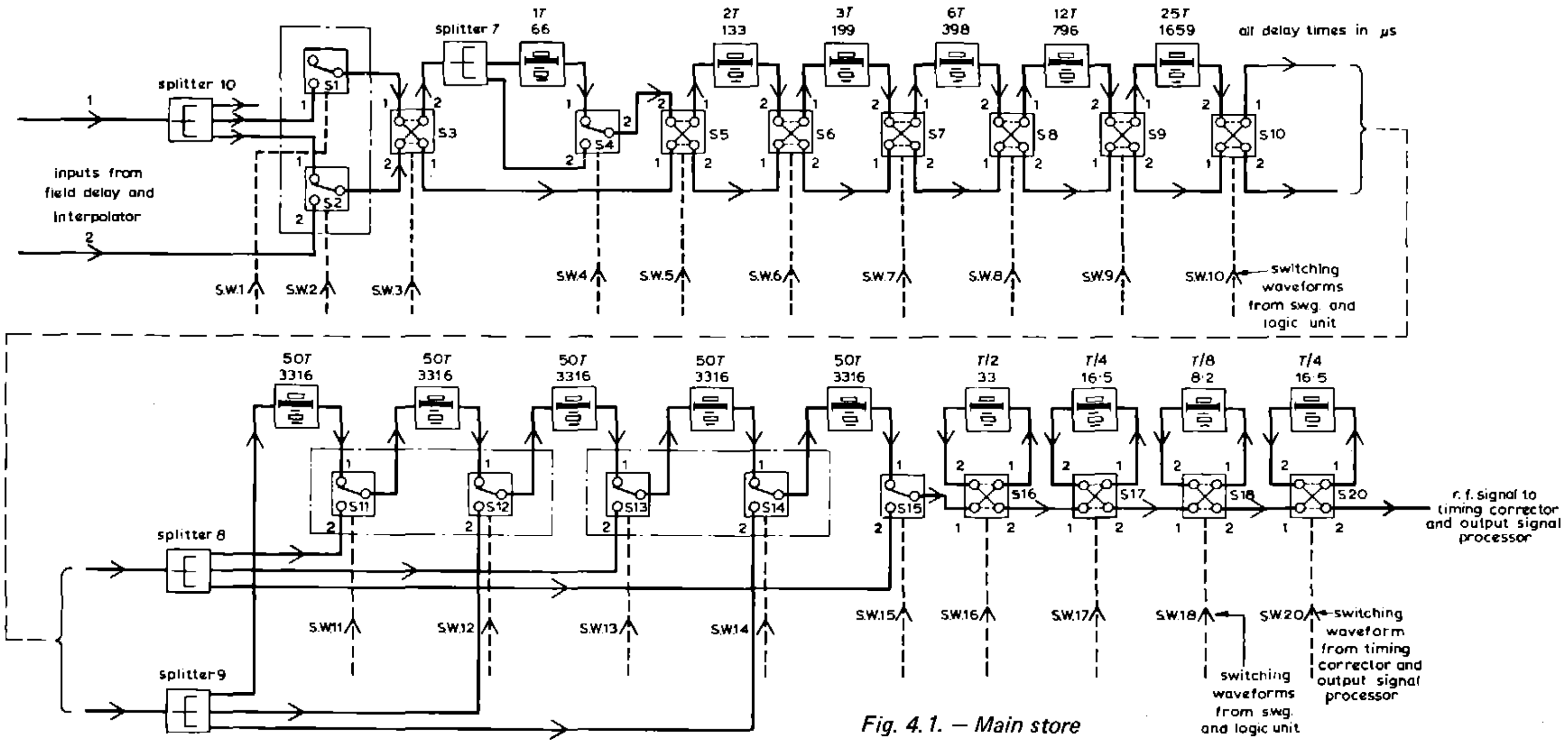


Fig. 4.1. – Main store

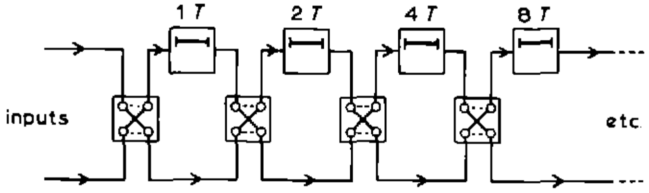


Fig. 4.2. – Binary delay cascade

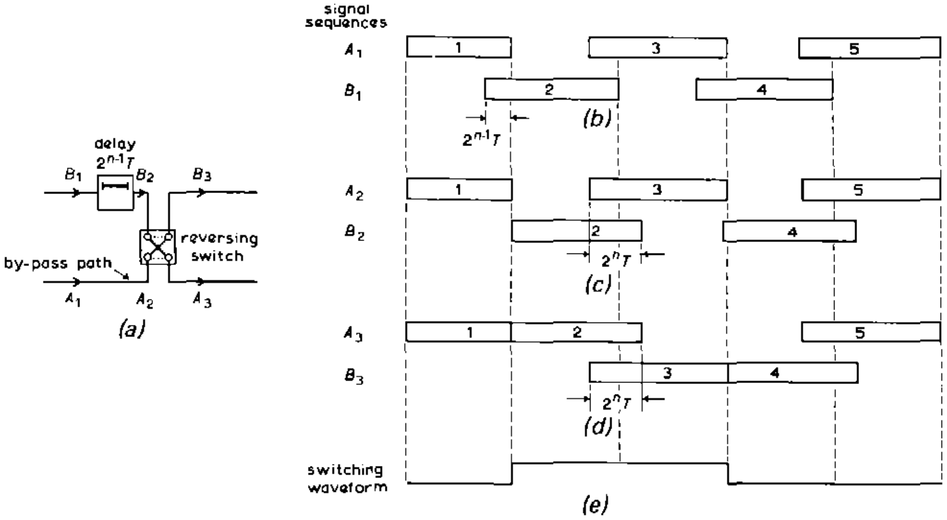


Fig. 4.3. – Action of binary delay store

At the first stage in the binary delay store (n = 1) the delay is $2^0 \times T$, i.e. equal to T, and the overlap between signals from the two paths is just one line; that extra line, in fact, which has to be inserted in the sequence. After the first stage alternate extra lines have been inserted into the sequence and the overlaps are now two units long. As each stage is traversed, the lengths of correctly related sequences and the overlaps between them are successively increased, until eventually complete sequences of output fields are built up, and the overlaps consist of unwanted information which can be discarded.

4.3. Modified-binary and tapped delay store

In practice, a store containing binary-related delay values has three main disadvantages. First, in the process described above, the discarded information forms a sequence $2^N T$ in duration which, with the value of T chosen, cannot be exactly equal to a field. Second, in considering the conversion in the reverse direction (625/50 to 525/60) it was thought desirable to use the same delay values, even though the total capacity required in the store would be different. Third, the longest delay values required for a binary-related delay store are too large to be manufactured as single quartz delays.

To overcome these disadvantages the modified store shown in Fig. 4.1 was evolved. The longest single delay is $50T$, i.e. approx $3^1/3$ ms. This is about the longest delay which can be manufactured at present; it is also both the difference between the input and output field durations and very nearly $^1/5$ of the input field duration. The close relationship of this delay value to the field durations at both standards simplifies the field-omission process which can be carried out by operations within the long delays alone and also allows conversion in the reverse direction to be based on the same set of delay values.

The shorter delay values used cannot, of course, form a binary set because 50 is not an integral power of two; however, by keeping as near to a binary set as possible, the action of the store is made reasonably simple. The values chosen, as shown in Fig. 4.1 are $1T$, $2T$, $3T$, $6T$, $12T$ and $25T$. The two outputs from these cascaded stages are at that point in the main store where signal overlaps equal in duration to $50T$ occur, and where correctly-ordered sequences with a duration of one field period have been generated. The $6T$, $12T$ and $25T$ stages are almost identical in action with those stages of a purely binary store. Generation of $6T$ overlaps in the $1T$, $2T$ and $3T$ stages is a more complicated process; this is fully described by Fig. 4.4 which, like Fig. 4.3, illustrates the progress of signals through the store.

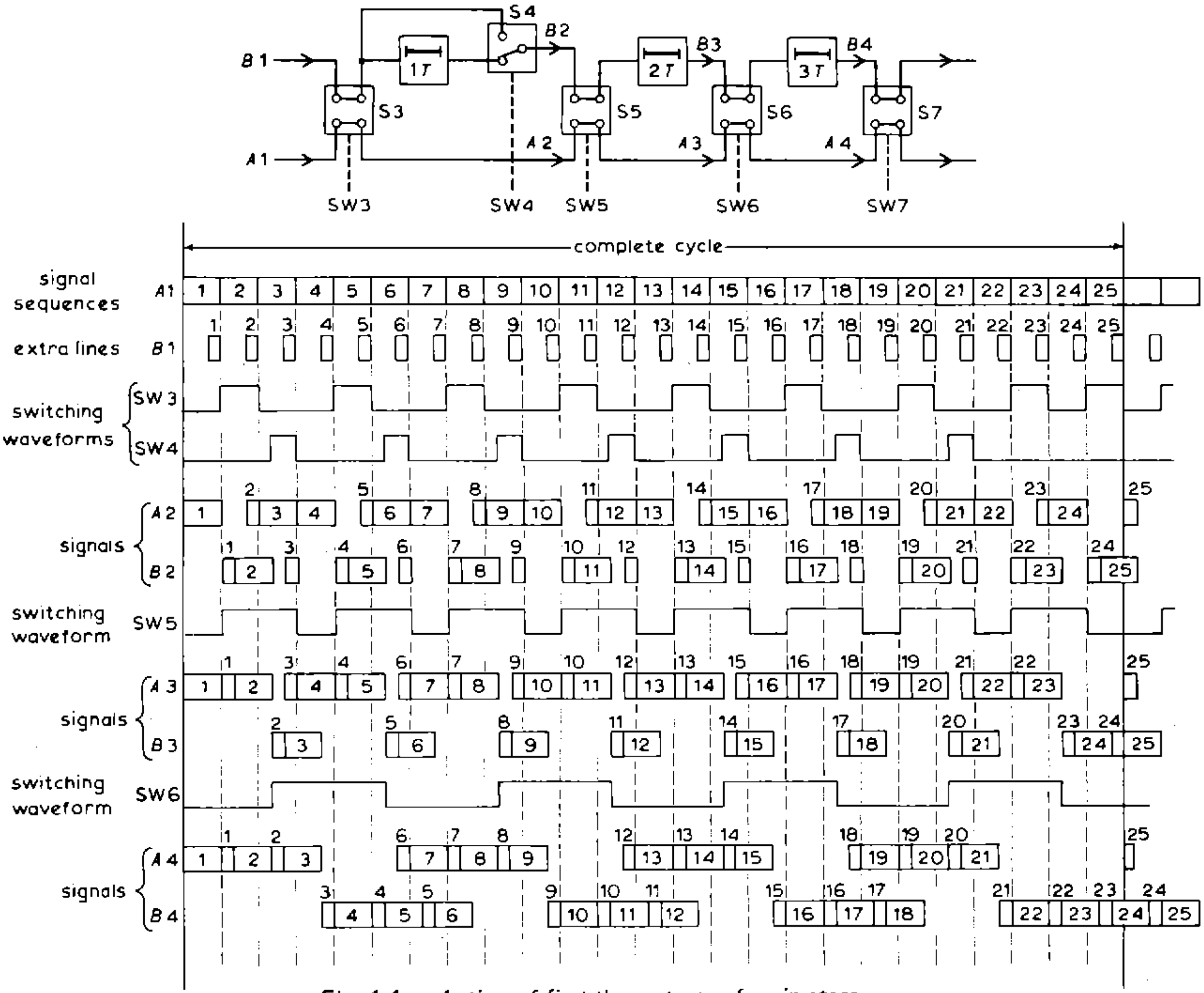
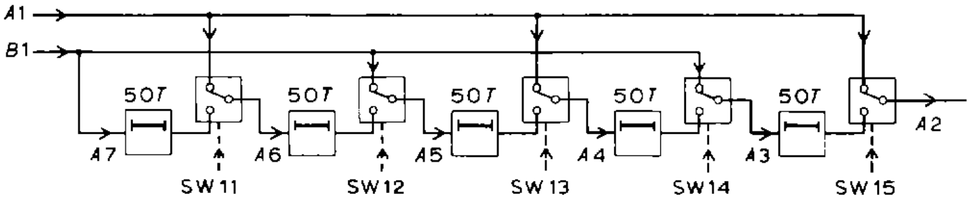
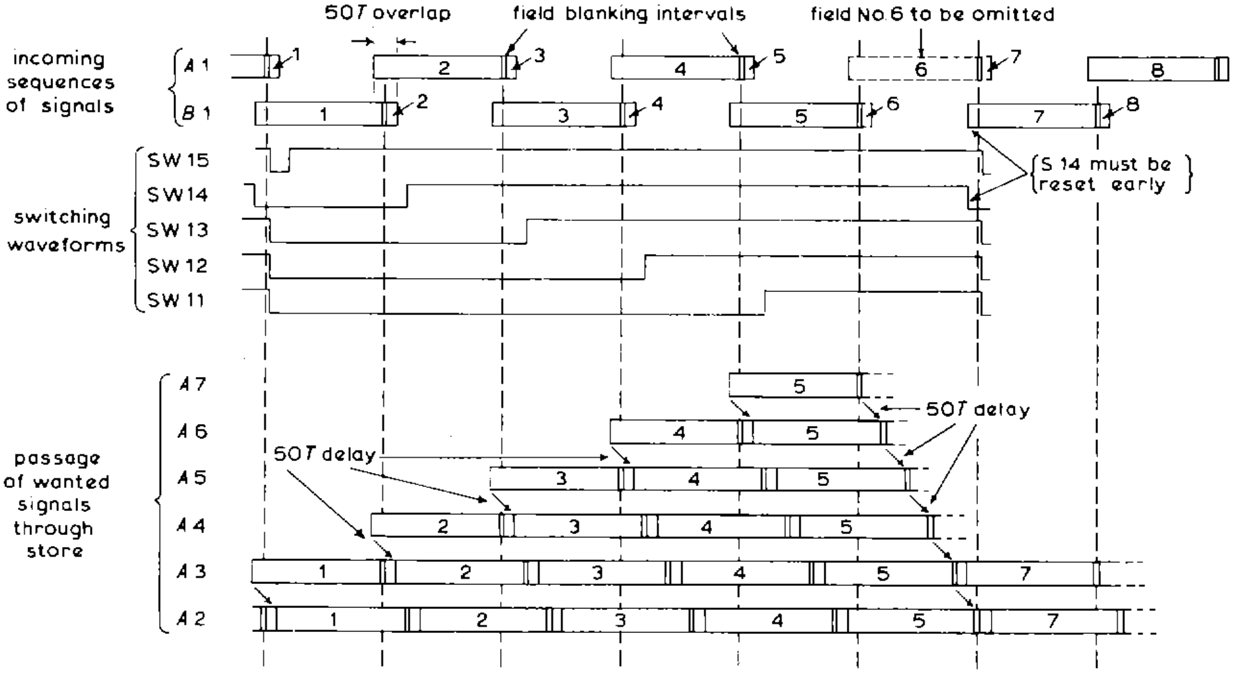


Fig. 4.4. – Action of first three stages of main store



(a)

Fig. 4.5(a) – Output section of main store



(b)

Fig. 4.5(b) – Action of tapped section of main store

The remaining five $50T$ delays are arranged as a tapped delay as shown in Fig. 4.5(*a*). Sequences of signals entering this section at two terminal points A_1 and B_1 as shown in Fig. 4.5(*b*), have been generated by complete cycles of increasing delay from $0T$ to $49T$ in the earlier modified binary sections and these sequences overlap each other by $50T$. Moreover, 50 units of delay are required for each input television field and each sequence contains a complete field of picture information. However, because the field frequencies of the 625 and 525 standards are not rigidly locked together, line signals at the beginning of each input field do not necessarily require zero delay and therefore the field-blanking intervals are assumed to occur at arbitrary positions in each sequence. In Fig. 4.5(*b*) fields have been numbered from 1 upwards, each field comprising a part of two successive sequences. The waveforms applied to switches S11 to S15 are shown together with the wanted signal sequences appearing at terminal points A_2 to A_7. The delays are switched into circuit progressively and are switched out of circuit together in order to discard field No. 6. It is necessary, however, to reverse S14 earlier than switches S11, 12, 13 and 15 to ensure that information for field No. 7 is stored in the first $50T$ delay in time for output following field No. 5.

4.4. Timing corrector extension

Following the $50T$ delays, four further short delays of durations $T/2$, $T/4$, $T/8$ and $T/4$ are included which can be switched into circuit by means of S16, S17, S18 and S20 (see Fig. 4.1). These are necessary to supplement the limited range of the following timing corrector. The first three delays, $T/2$, $T/4$ and $T/8$ are switched into or out of circuit during the field-blanking intervals according to the relative timing of fields in the 625/50 and 525/60 standards thereby reducing the timing errors to within about 15 μs in practice. The additional $T/4$ delay (of 16·5 μs duration) is available for 525/60 monochrome operation when the field frequency is nominally 60 Hz i.e. one part in 1000 less than that for colour operation. The delay can be switched into circuit during the active field whenever the timing corrector capacity is about to be exceeded.

5. Logic unit

5.1. General

The conversion process is controlled by the logic unit which is constructed using transistor buffer-stages and 148

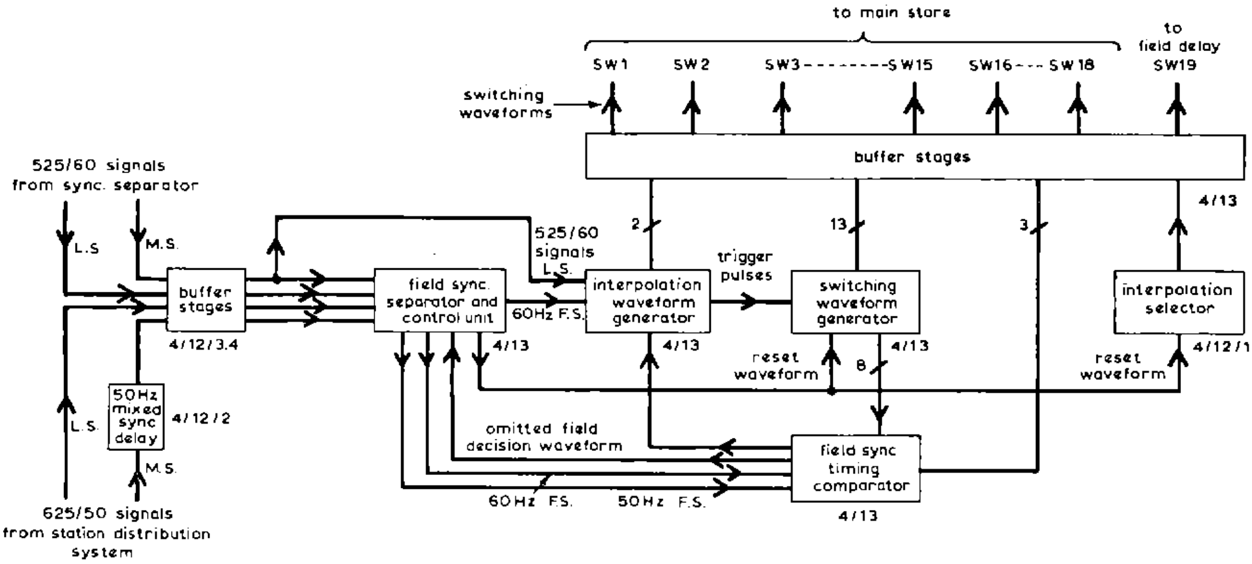


Fig. 5.1. – Switching waveform generator and logic unit schematic

integrated circuit packages containing 418 active RTL* logic gates and J-K flip-flops.

The five main units are connected as shown in the outline block diagram, Fig. 5.1. The selection of television lines in the interpolation process is controlled by waveforms SW1 and SW2 generated by counting input (525/60 standard) line syncs in the interpolation waveform generator. Trigger pulses coincident with the times of extra lines are transmitted to the switching-waveform generator which produces switching waveforms SW3 to SW15 to control the increase of delay in the main store.

In order to allow slave-locking of the converted output (625/50 standard) signal, the processes of interpolation and delay-increase in the main store are interrupted during the field-blanking intervals. Mixed syncs at the two standards are fed to the field-sync-separator and control unit which thereby generates field-timing pulses for application to the field sync timing comparator. Here, the exact delay required at the time of occurrence of each input field sync is determined and, if a change is necessary, the main store delay value is corrected by the transmission of a suitable number of trigger pulses to the switching-waveform generator during the field-blanking interval. At the same time (during the field-blanking interval), switching waveforms SW16 to SW18 are derived to control the timing-corrector extension (see Section 4.4). An output from the field-timing comparator is also used to determine when to discard a field; at such times a re-set waveform, (provided by the field-sync-separator and control unit), is fed to the switching-waveform generator and thence to switches to S11 to S15 in the main store, thereby reducing the total delay by 250*T*. This re-set waveform is also fed to the interpolation selector to control the operation of S19 as required for movement interpolation.

The actions of the interpolation-waveform generator and switching-waveform generator are now explained in more detail.

5.2. Interpolation and switching-waveform generators

Two alternative pairs of switching waveforms, SW1 and SW2, are shown at the top of Fig. 5.2. Two pairs are necessary because of the field-omission process which interrupts the regular flow of odd and even fields. In any one five-field cycle, even-numbered output fields are generated at the time of even input fields, whereas in the next five-field cycle even output fields are generated at the time of odd input fields. This implies a change in the line-selection process, controlled by SW1 and SW2 and thus the alternative waveform pairs are selected in alternate five-field cycles.

Waveform SW1 determines the extra lines generated and is used also as a trigger waveform to control the increase of delay in the main store. Switching waveforms SW3 to SW10, shown in Fig. 5.2, on a contracted scale, are generated by counting processes in the switching-waveform generator. The action of the main store was explained in the previous section and SW3, SW4 and SW5 are identical with the waveforms shown in Fig. 4.4. A difficulty arises in that each waveform determines the places in the input signal where a switch changeover has to take place; however, the actual operation of the switch must be delayed until the appropriate signal has traversed the delays in the main store to reach that switch. Some of the switching waveforms are therefore delayed and the required delay for each waveform, as indicated in Fig. 5.2 by the broken lines, is obtained by counting the appropriate number of cycles of a crystal oscillator.

Waveforms SW11 to SW15 which control the tapped-

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* RTL (resistor-transistor logic) is used here since the maximum required speed of operation is only about 2 MHz.

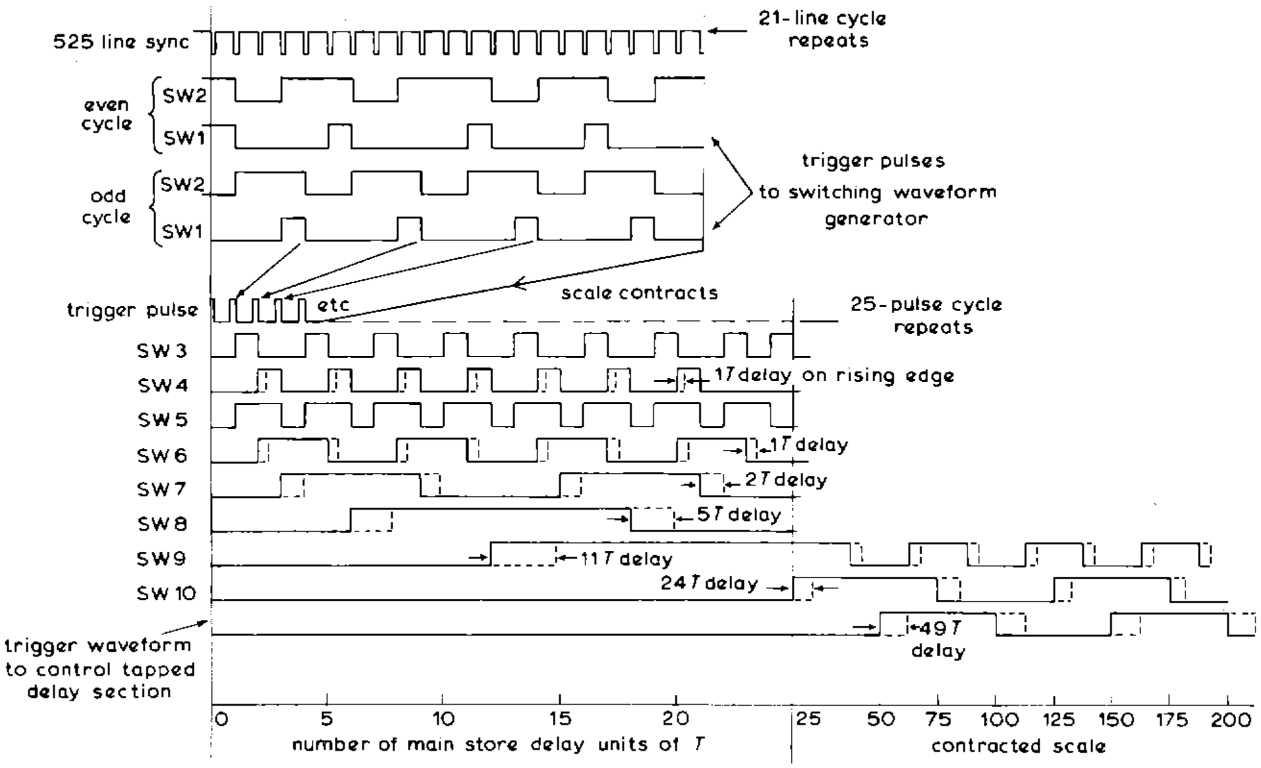

Fig. 5.2. – Waveforms from interpolation and switching waveform generators

delay section of the main store are also generated in the switching-waveform generator. The sequential operation of switches S11 to S15 in the tapped-delay section of the main store (see Fig. 4.5) is initiated by the trigger waveform shown at the bottom of Fig. 5.2.

The action described above continues throughout each active 525/60-input field and ensures that the active signals are interpolated and delayed correctly to form active output fields on the 625/50 standard.

During each input field-blanking interval, the control of delay is passed to other units by interrupting the flow of trigger pulses from the interpolation-waveform generator to the switching-waveform generator; four trigger pulses are omitted each time. In these intervals, the switching-waveform generator is supplied with trigger pulses from a separate source, a sufficient number of pulses being gated through to keep the main store output signal in step with the 625/50 output sync pulses. The number of pulses required for this purpose is dependent on the rate of change of field-phase between the input and output scanning standards and is between three and six in practice. However, after a signal interruption (or when first receiving an input signal), up to twenty pulses are available so that the main store delay is established at the correct value in as short a time as possible. This action ensures minimum disturbance to the output picture.

The required delay to be set in the main store is determined at the time of each input 525/60 field sync pulse, by measuring the time elapsed from the previous 625/50 output field sync pulse and subtracting this value from the known 625/50 field duration, this being a prediction of the time interval between one input field sync pulse and the next output field sync pulse. In practice, a counter is set to a value corresponding to the output 625/50 field duration. Subsequently, counting starts at the time of an output 625/50 field pulse and continues until the next input 525/60 field pulse; a negative direction of count is used to simulate subtraction. For convenience, the counter operates according to the same code as the switching-waveform generator and at such a rate as to count exactly 128 pulses during a time equal to the main store T unit. Thus, at the time of each input field pulse the counter determines the setting required for each stage of the switching-waveform generator (and hence the delay value in the main store); this information is held in a part of the counter termed Register A. Further, the subdivisions given in the early stages of the counter determine subdivisions of the T unit which are used to control the short delays forming extensions to the timing corrector via a subsidiary register (Register B).

The value standing in the counter at the time of the 525/60 input field pulse is first used to determine whether or not the next input field is to be discarded. The top two lines of Fig. 5.3 show relative timings of input and output

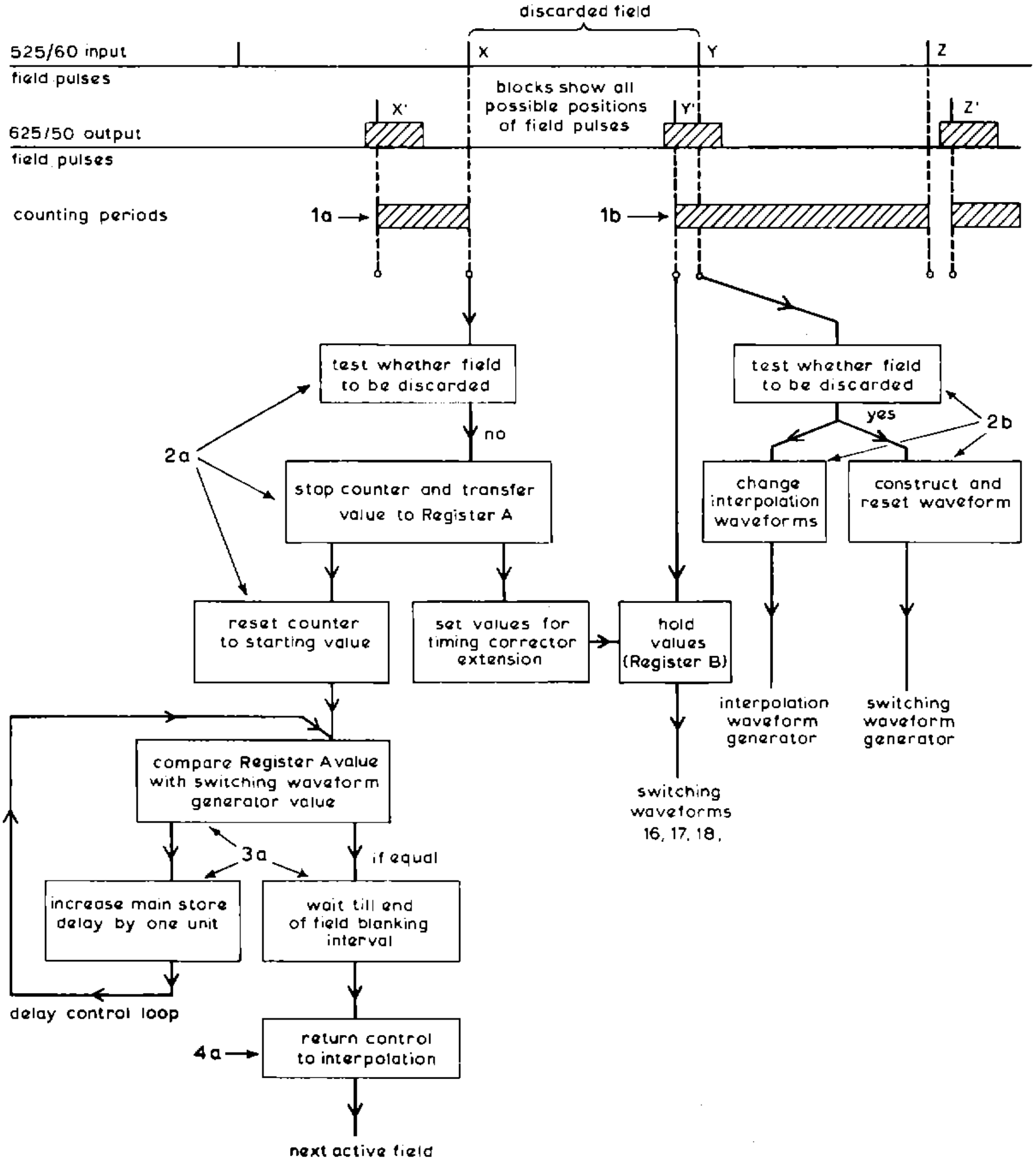
discarded field
525/60 input
field pulses
X
Y
Z
blocks show all possible positions of field pulses
X'
Y'
Z'
625/50 output
field pulses
counting periods
1a
1b
test whether field to be discarded
no
2a
stop counter and transfer value to Register A
reset counter to starting value
set values for timing corrector extension
hold values (Register B)
compare Register A value with switching waveform generator value
3a
if equal
increase main store delay by one unit
wait till end of field blanking interval
delay control loop
4a
return control to interpolation
next active field
test whether field to be discarded
yes
2b
change interpolation waveforms
construct and reset waveform
interpolation waveform generator
switching waveform generator
switching waveforms 16, 17, 18,

Fig. 5.3. – Flow diagram of field-phasing logic

field pulses. The 625/50 output pulses are shown as blocks which indicate all the possible positions which they could occupy assuming that the input field shown was the one to be discarded. The decision whether or not to discard a field depends, as can be seen in Fig. 5.3, on whether the counter value is greater than or less than a number near 250 T-units. The exact value chosen in practice must lie between 251·5T and 255·5T. A value less than 251·5T is too small because the wanted field immediately after the discarded field will require a delay less than zero, whereas a value greater than 255·5T is too large because the wanted field immediately before the discarded field will require a delay greater than the available capacity of the store. The action of the logic unit differs according to the decision whether or not to discard the next field and is outlined in Fig. 5.3 as a 'flow diagram'. The successive blocks indicate the sequence of events all of which occur during the field blanking interval.

The sequence of operations occurring when a field is not discarded (starting at the 625/50 output field pulse marked X') is as follows:

(1a) X' – counter starts; active field interpolation in progress

(2a) X — input field blanking commences, interpolation ceases. Counter value is tested; result: — this field not to be discarded. Stop counter and transfer value to Register A. Reset counter. At the next output field sync pulse, transfer timing-corrector-extension values from the early stages of Register A to Register B.

(3a) X + 3 lines (approx.) — Commence transmitting pulses (30 kHz is used as being sufficiently frequent) to switching-waveform generator and continue until the setting matches that of Register A.

(4a) X + 21 lines — end of field blanking interval. Return to interpolation etc.

The sequence of operations occurring when a field is discarded (starting at the 625/50 output field marked Y′) is as follows:

(1b) Y′ — counter starts; active field interpolation in progress

(2b) Y — input field blanking commences, interpolation ceases. Counter value is tested; result: — this field to be discarded.
(N.B. Counter is not stopped in this instance).
Generate pulse to change interpolation phase.
Initiate construction of re-set waveform to control tapped delay section of main store.

(1c) Z — as (2a) etc.

As can be seen from the above description, the necessity for the locking facility considerably complicates the action of the logic unit and during the design and development, several difficulties arose. The following notes outline these difficulties and the means whereby they were overcome.

(1) Waveforms in Fig. 4.5(*b*) show that S11, S12, S13 and S15 are re-set at the time of an output (625/50) field pulse whereas the re-set time for S14 is about 1 ms before an input (525/60) field pulse following a discarded field. The way in which this is achieved represents the solution to problems in logic arrangement, the subject of which is outside the scope of this report.

(2) To determine the exact interval between output and input field pulses it is necessary to measure the elapsed time between appropriate line sync pulses and not between field sync pulses (because, for odd fields, the field sync occurs half way between adjacent line sync pulses). The particular line sync pulses used change every five fields. For one five-field sequence, the appropriate line syncs are those immediately following the field syncs; in the alternate five-field cycles, however, the line sync pulses occurring one line later are used.

(3) In Fig. 5.3 the block defining all possible Y′ positions of output (625/50) field sync pulses shows that the occurrence of such a pulse immediately after an input (525/60) field pulse is permitted as an extreme condition. But, in this event, the next field will initially require more than 50 *T*-units of delay. Therefore, because the re-set process (normally) removes all 50*T* delays from circuit, it was necessary to arrange that pulses operating in the delay control loop during the field blanking interval are delayed so that they act after re-setting has occurred thus changing the delay from, say, 48*T* through 50*T* to the required value of 51*T*.

6. Timing corrector, transcoder and output signal processor

6.1. General

The purpose of the timing corrector and output signal processing section of the converter is to derive a standard 625/50 output video signal from the intermediate video signal obtained from the main store. A simplified block diagram of this section is shown in Fig. 6.1 and a more detailed diagram is shown in Fig. 6.7.

Two output signals are provided. The output signal provided by the PAL coder gives a normal PAL signal during colour operation but subcarrier is removed during monochrome operation. The purpose of the 'mono only'

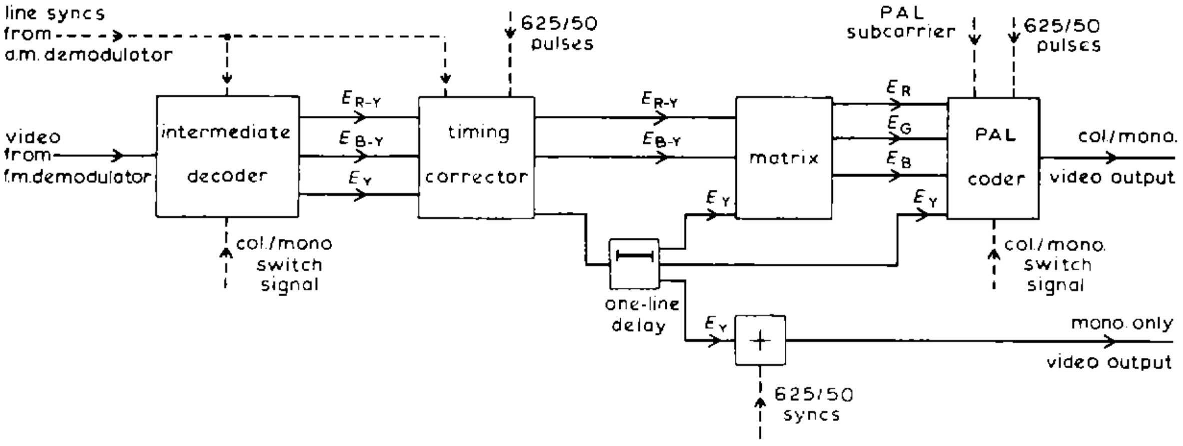

Fig. 6.1. — Output transcoder

output signal was to provide a signal which never contained colour subcarrier, for further conversion to the 405-line standard; this output is not now used since all BBC networks carry 625-line signals and conversion to 405-lines takes place at the transmitters. As shown in Fig. 6.1, the intermediate video signal is first decoded into its luminance and two colour-difference components. These three signals are then fed to the modified line-store timing corrector which acts as a variable delay, ranging from zero to approximately 26 µs and removes irregularities in the timings of the television lines fed from the main store. Each television line is 'written-in' to the line-store at the time it is received from the main store and is 'read-out' at a time controlled by the local synchronising pulses. The main form of timing irregularity removed by the timing corrector is illustrated in Fig. 6.2. This figure represents a television display of the input signal to the timing corrector, using the output (local) 625/50 synchronising pulses, to lock the monitor. The serrated effect at the sides of the raster arises because the line period is, in general, the same as that of the 525/60 input signal to the converter, i.e. 63·5 µs, but every 5th or 6th line blanking interval is extended to give a mean line period identical to that of the 625/50 output signal, i.e. 64 µs.

The three output signals from the timing corrector are matrixed together to form R, G and B colour signals which are then fed, together with a separate luminance signal, to the output PAL coder. By operating this coder in its '4*T*' position, only the R, G and B signals contribute to the chrominance component of the output signal. During monochrome operation, a relay disconnects the output of the chrominance unit, with the result that the R, G and B signals are rejected and the colour burst is removed from the output signal.

The purpose of the one-line delay in the luminance path to the PAL coder is to correct a one-line vertical misregistration between chrominance and luminance which would otherwise appear on pictures received from the converter. This misregistration is due partly to comb-filtering of the NTSC input signal and partly to the decoding action of the PAL receiver. Both these devices incorporate a one-line delay and their chrominance outputs are the mean value of the chrominance amplitudes on two successive lines; as a result, each gives a ½-line vertical misregistration.

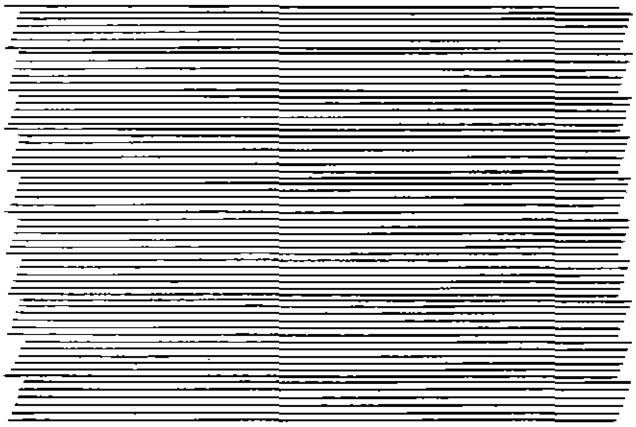

Fig. 6.2. – Output raster without timing correction

The intermediate decoder and timing corrector will now be described in more detail.

6.2. Intermediate decoder

A block diagram of the intermediate decoder is shown in Fig. 6.3. This unit decodes the intermediate video signal into its luminance and two colour-difference components.

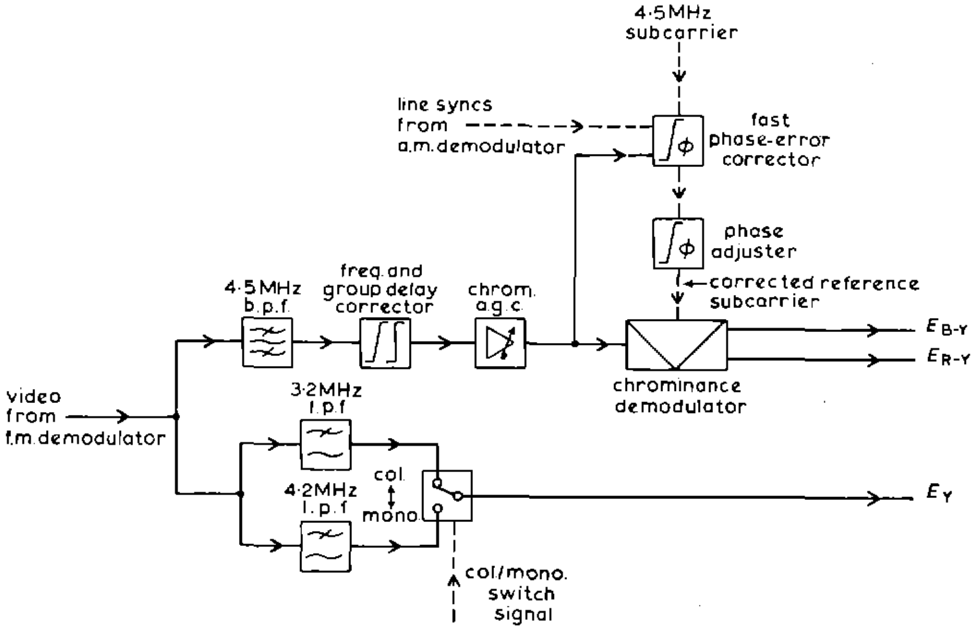

Fig. 6.3. – Intermediate decoder

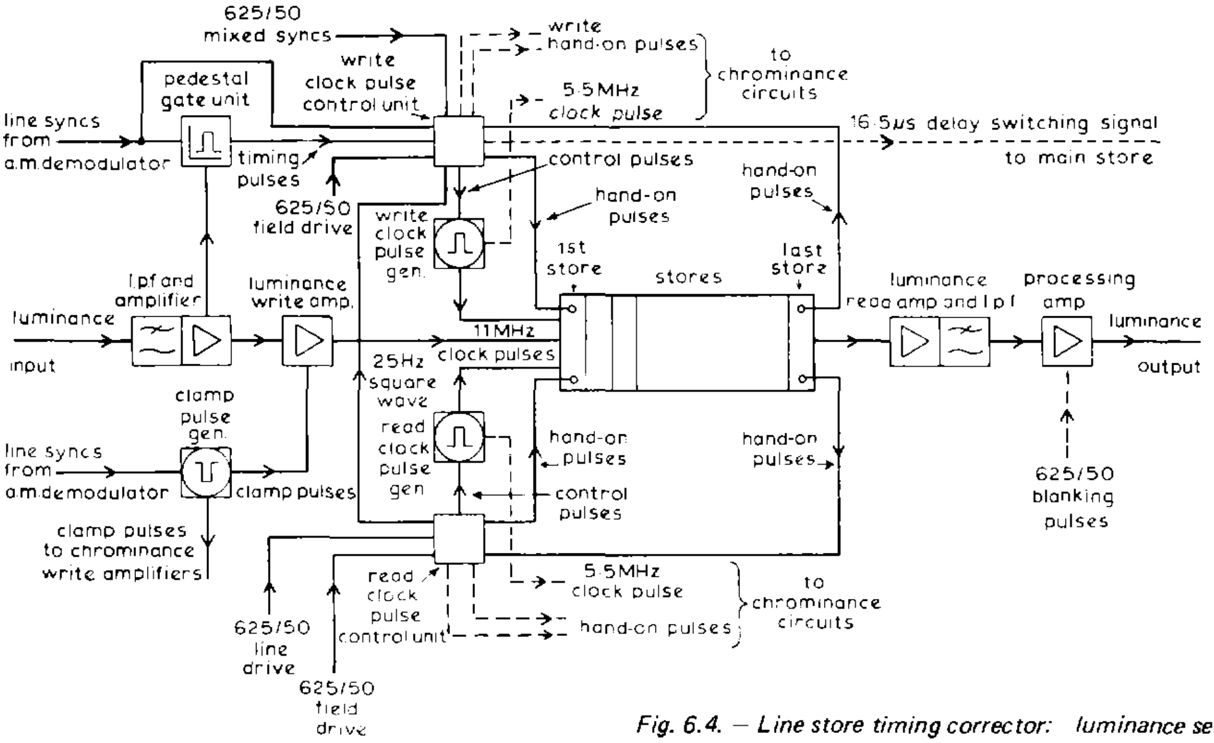

Fig. 6.4. – Line store timing corrector: luminance section

During colour operation, the luminance and chrominance components of the intermediate signal are separated by means of a 3·2 MHz low-pass filter and a band-pass filter centred on 4·5 MHz. For monochrome operation, the 3·2 MHz low-pass filter is replaced by a 4·2 MHz low-pass filter and any signals decoded by the chrominance section are rejected in the PAL coder at the output of the converter. The colour/monochrome switching signal which selects the appropriate low-pass filter is obtained from the burst-detector in the NTSC decoder at the input of the converter. The luminance signal obtained from the colour/monochrome switch is fed directly to the timing corrector.

The chrominance section of the intermediate demodulator is rather more complex than the chrominance section of an NTSC or PAL decoder. There are two reasons for this complexity:

(a) The signal path through the main store of the converter changes systematically as varying delays are introduced and these changes in the signal path cause small line-to-line variations in the amplitude of the intermediate subcarrier. These variations are removed by the chrominance a.g.c. unit, which uses the amplitude of the burst as a reference to control a variable gain amplifier. The chrominance a.g.c. is discussed in more detail in Section 7.2.

(b) The irregularities in signal timing result in discontinuities in the phase of the colour subcarrier and it is therefore necessary to feed the chrominance demodulators with a special reference subcarrier which is adjusted in phase at the beginning of each line. This process is performed in the fast phase-error corrector, in which the phase of the reference 4·5 MHz subcarrier is suitably adjusted by comparison with the phase of each burst (the burst and its associated line signal suffer the same phase changes having travelled by the same path through the converter). The fast phase-error corrector is described in Section 7.3.

The phase-corrected subcarrier is fed to the chrominance demodulator via a phase adjuster which is only altered during initial setting up procedures and acts as an overall hue control.

The chrominance demodulator unit is similar to that used in NTSC decoders except that it requires an external reference subcarrier.

Finally, the luminance and colour-difference signals are fed to a matrix in the luminance unit to form the R, G and B signals. This unit is placed after the timing corrector so that timing correction has only to be performed on one wideband and two narrow-band colour-difference signals rather than on the three wideband R, G and B signals.

6.3. Line-store timing corrector

6.3.1. General

The corrector is divided into three similar sections; one section handles the luminance component of the video signal and the other two sections handle E_{R-Y} and E_{B-Y} colour-difference signals. Also included in the timing corrector is the 16·5 μs logic unit, the function of which is described in Section 6.3.4.

The general principle of operation of each section is similar to that of a line-store standards converter,[13,14,15] except that no interpolation is used.

For a block diagram of the complete timing corrector, the reader is referred to Fig. 6.7.

6.3.2. Luminance section

A block diagram of this section and associated signal waveforms are shown in Figs. 6.4 and 6.5.

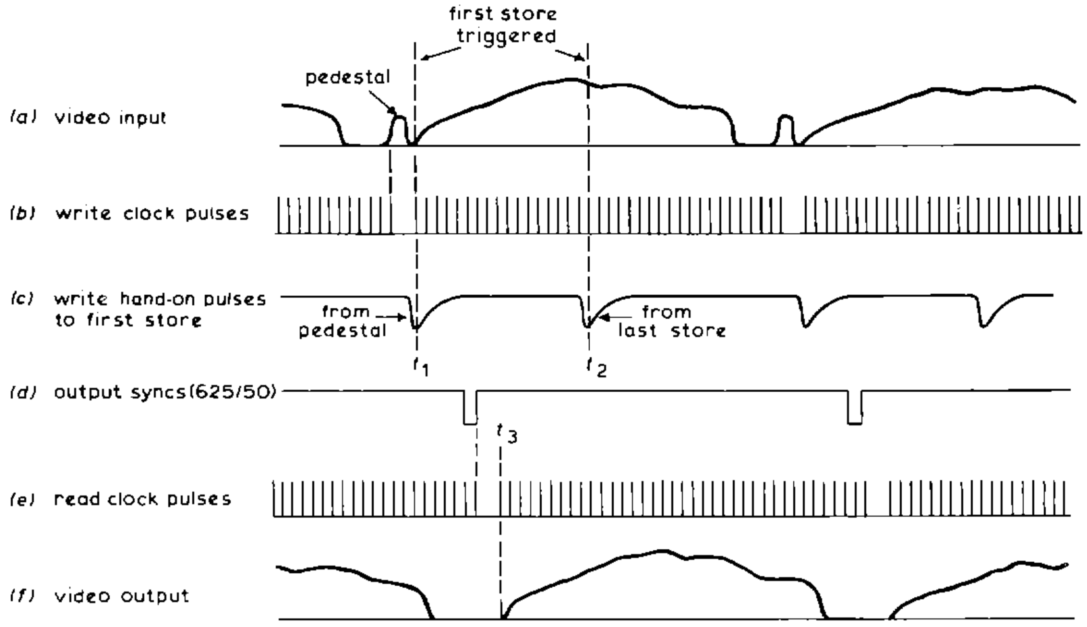

Fig. 6.5. – Timing corrector waveforms

The luminance input signal is fed to all store-boards via a low-pass filter and the luminance-write amplifier.

This input signal is also fed to the pedestal-gate unit in which the leading edge of the pedestal (see Fig. 6.5(*a*)) is gated-out, using syncs from the a.m. demodulator. The pulse obtained from the pedestal-gate is used to initiate the writing sequence by generating the following signals in the 'write' clock-pulse control unit:–

(a) A clock-pulse blanking signal which is used to stop the 'write' clock-pulse generator in the interval between the leading edge of pedestal and the start of picture information (see Fig. 6.5(*b*)).

(b) A 'hand-on' pulse which is fed to the first store board and occurs immediately prior to the first 'write' clock-pulse (see Fig. 6.5(*c*)).

The hand-on pulse opens a gate on the first board and allows the first 'write' clock-pulse to trigger the sampling-pulse generator on the first board. The first board thus samples and stores the magnitude of the luminance signal at the time of the first clock-pulse.

The sampling-pulse generator on the first board also generates its own hand-on pulse which is fed to the next board in the chain. In this way the second clock-pulse is allowed to trigger the second board and so on until the last board in the chain is reached.

The clock-pulse frequency is adjusted so that the triggering of the last board occurs half way through each line period. In order to sample the second half of each line period, the sampling cycle is now repeated starting at the first board again. This second sampling cycle is initiated by feeding the hand-on pulse from the last board back to the first board via the clock-pulse control unit. The clock-pulse control unit ensures that the cycle can only be repeated once per line period.

The process of 'reading-out' the stored samples is very similar to the writing process. The 'read' clock-pulse blanking and hand-on pulse to the first board are derived from the 625/50 output standard sync pulses. The signal that is read-out is therefore appropriately timed with respect to these sync pulses (see Fig. 6.5(*d*) (*e*) and (*f*)).

Since each board is used twice per line period, it is essential that the first 'read' clock-pulse should occur during the interval between the two times in a line period at which information is written into the first board, i.e. t_3 in Fig. 6.5(*e*) should occur between t_1 and t_2 in Fig. 6.5(*c*). The interval of time from t_1 to t_2 in fact determines the available range of timing correction.

In the explanation given above, it is evident that if the initial hand-on pulse to the first store board always occurs immediately before the first clock pulse (which is coincident with the start of the picture information), then the nth picture element will always be sampled by the nth store board. As a result of small differences in the transfer characteristic of individual boards, such a repetitive sampling pattern causes visible stripes on the output picture; these stripes are vertical because the nth picture element in any line is directly below the nth element in the preceding line.

The visibility of the stripes is reduced (by about 3 dB) by arranging that, on alternate fields, the initial hand-on pulse to the first board occurs immediately before the third clock pulse instead of before the first. Thus, the nth picture elements in all lines of one field are sampled by the nth store board, whereas the nth elements of lines in the following field are sampled by the (n+2)th board.

Obviously, because the first clock pulse is coincident with the start of each line of picture information, the shifting storage pattern described above causes the first two picture elements in lines of alternate fields to be ignored. By arranging that the missing elements occur during the line-blanking interval, the effect of this loss is not visible in the output picture.

The alternating time-displacement of hand-on pulses occurs for the reading as well as the writing process so that the correct line spatial relationships are maintained. The necessary field-rate control signals are derived in the two clock-pulse control unit from feeds of field-drive pulses.

6.3.3. Colour-difference section

A block diagram of one of these sections is shown in Fig. 6.6. The colour-difference sections are similar to those in the luminance section except that sampling occurs at one half the frequency. Each colour-difference path therefore contains half the number of stores in the luminance path and the clock-pulse frequency is one half the luminance clock-pulse frequency.

The hand-on pulses to the first boards in the colour-difference paths are obtained from the same source as those for the first luminance boards. Hand-on pulses from the last colour-difference boards are therefore not used.

6.3.4. 16·5 µs logic unit

The purpose of this unit (shown on Fig. 6.7) is to control the switching of a 16·5 µs delay line in the main store which increases the range of timing correction by 16·5 µs. This extra range is only required for those monochrome signals which have a field frequency of approximately 60·00 Hz and is not required when the field frequency is 59·94 Hz, as used for colour. The extra delay is inserted in signal path when the time interval $t_3 - t_2$ shown in Fig. 6.5 becomes less than approximately 2 µs. Once the delay has been switched into the circuit it remains switched-in until the beginning of the following field period, when it is automatically replaced by a straight-through path.

7. Aspects of special interest

7.1. Theoretical considerations of interpolation between f.m. signals

Frequency-modulation is used in the field store standards converter to reduce the effect of gain inequalities in the delay-units as they are switched in and out of the signal path. However, interpolation requires the weighted addition of the video signals on successive lines and fields. For this reason, and to avoid demodulation and remodulation, an averager was developed which would, if presented with instantaneous frequencies f_1 and f_2, produce at its output a constant amplitude carrier of frequency $(f_1 + f_2)/2$, thereby averaging the modulations of the inputs.

The simplest way of averaging two frequencies is to mix the two (f_1 and f_2) in order to produce their sum $(f_1 + f_2)$ and then to halve this to obtain the average $(f_1 + f_2)/2$. Since the two frequencies are close, however, a mixer that produces harmonics (a bridge ring-modulator, for example) would be unsuitable; the second harmonics of the input frequencies would be inseparable from the required sum frequency.

A device that produces only half-sum and half-difference frequencies can be made simply by adding the two signals (A at f_1 and B at f_2) at the same amplitude. The result of this is a frequency $(f_1 + f_2)/2$, amplitude-modulated at a frequency $(f_1 - f_2)/2$ as can be seen in Fig. 7.1(*a*).

This is shown in the trigonometric identity:

$$E\sin\omega_1 t + E\sin\omega_2 t = 2E\sin\frac{(\omega_1+\omega_2)}{2}t\ \cos\frac{(\omega_1-\omega_2)}{2}t$$

Similarly, if the signals A and B are subtracted, the same

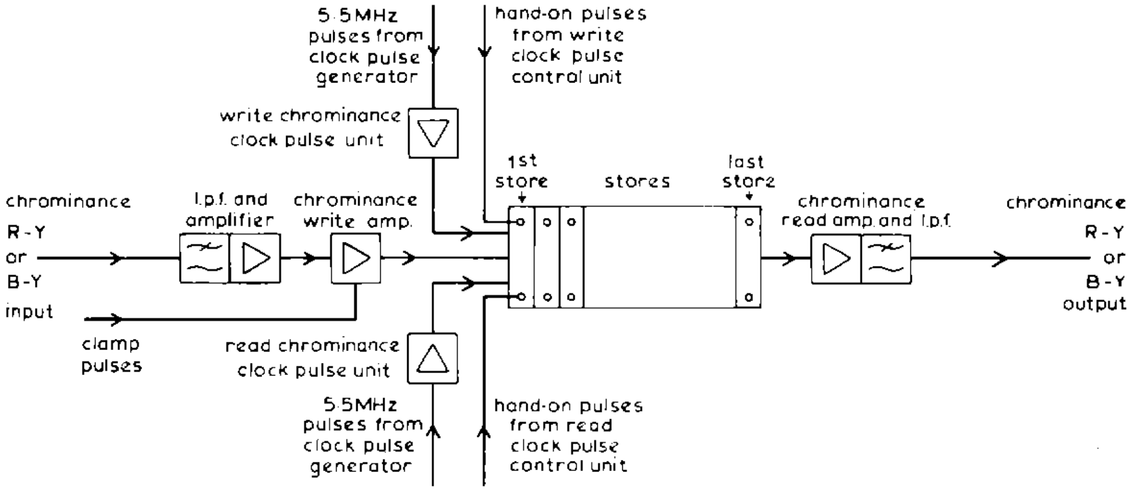
5·5MHz pulses from clock pulse generator
hand-on pulses from write clock pulse control unit
write chrominance clock pulse unit
1st store
stores
last store
chrominance R-Y or B-Y input
l.p.f. and amplifier
chrominance write amp.
chrominance read amp. and l.p.f.
chrominance R-Y or B-Y output
clamp pulses
read chrominance clock pulse unit
5·5MHz pulses from clock pulse generator
hand-on pulses from read clock pulse control unit

Fig. 6.6. – Line store timing corrector: one of the colour-difference sections

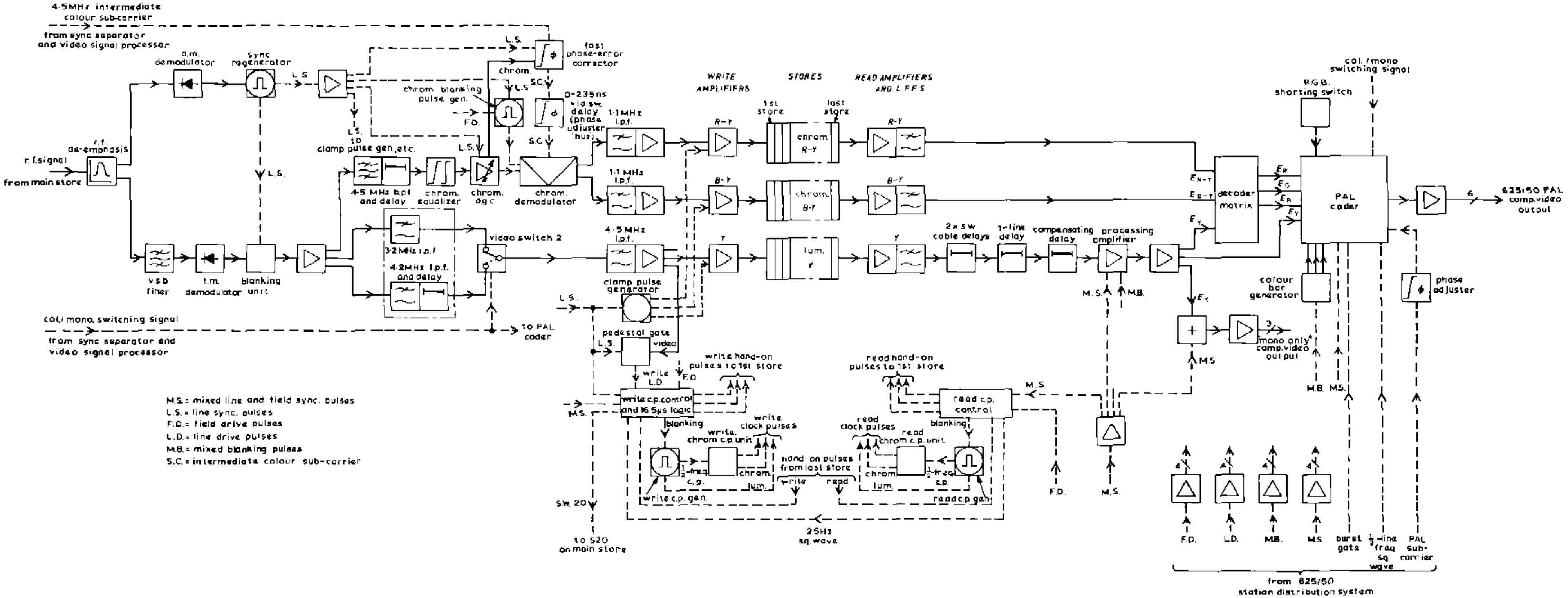

Fig. 6.7. – Output demodulator: timing corrector and transcoder

frequencies result but the signals are in quadrature with the corresponding signals from the addition, as shown in the identity:—

$$E \sin \omega_1 t - E \sin \omega_2 t =$$

$$= 2E \cos \frac{(\omega_1 + \omega_2)}{2} t \sin \frac{(\omega_1 - \omega_2)}{2} t$$

In both cases the wanted $(f_1 + f_2)/2$ component suffers a phase reversal at every zero-crossing of the $(f_1 - f_2)/2$ component (see Fig. 7.1(*a*)), but full-wave rectification may be employed to remove this — a process that also doubles the fundamental frequency, producing $(f_1 + f_2)$ (Fig. 7.1(*b*)).

Although the signals after rectification are of unchanging phase they are still 100% amplitude modulated. However, the $(f_1 + f_2)$ component resulting from the subtraction of the signals is in quadrature with that from the addition, so that if the two rectified waveforms |A + B| and |A − B| are subtracted, the wanted $(f_1 + f_2)$ frequency remains — with much of the amplitude modulation removed (Fig. 7.1(*c*)).

Unwanted frequency components introduced in the rectification stages can be filtered out and the remaining amplitude modulation is easily removed by a limiter (Fig. 7.1(*d*)). Fig. 3.1 shows the location of the separate screened units which constitute the complete F.M. averagers.

The mixer described above produces the sum of the two input-frequencies rather than the average. Consequently, it is necessary to divide the resulting frequency by two. This may theoretically be done either before or after the addition of the two frequencies. In practice, it is done

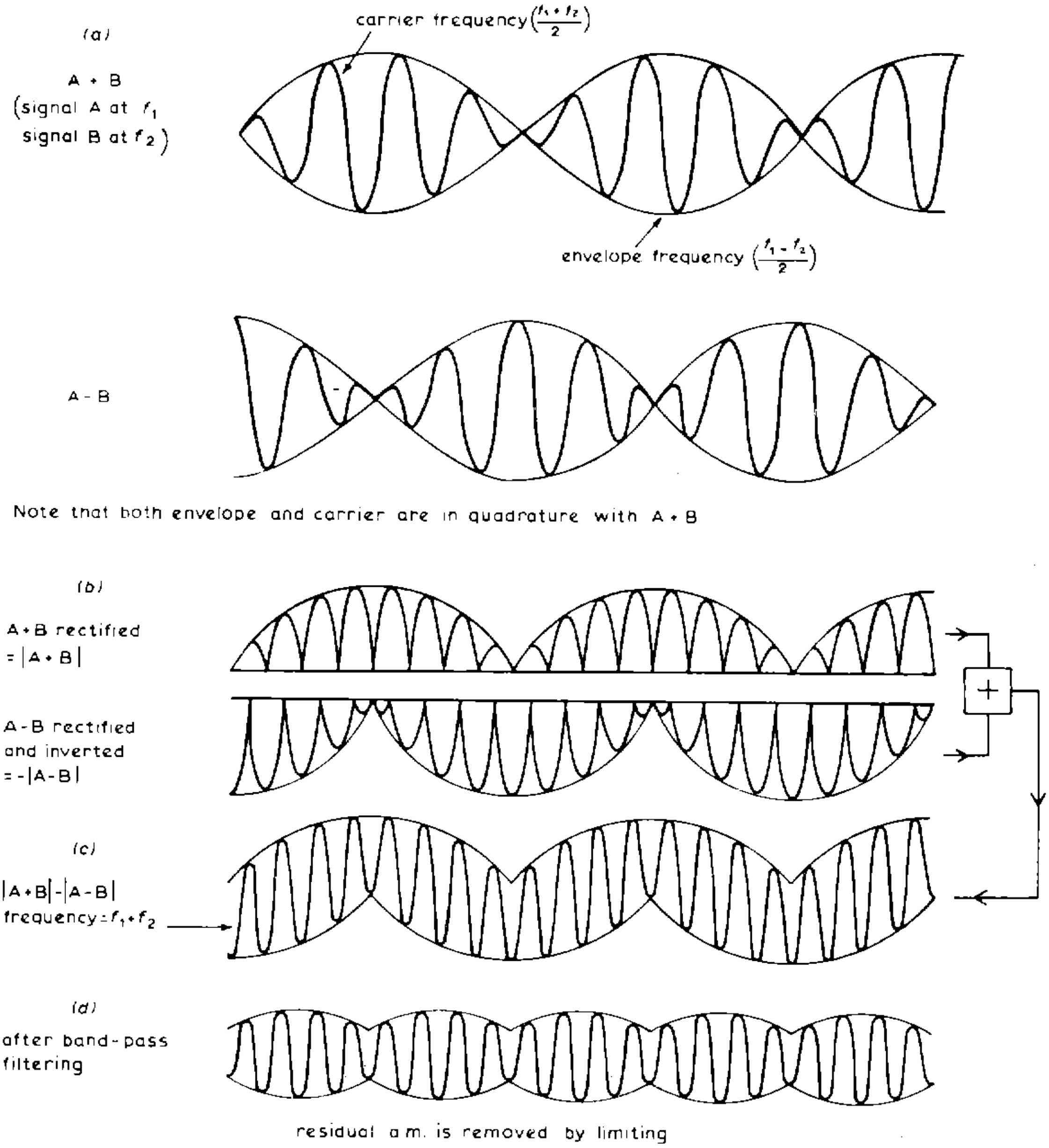
(a)
A + B
(signal A at f_1
signal B at f_2)
carrier frequency $\left(\frac{f_1 + f_2}{2}\right)$
envelope frequency $\left(\frac{f_1 - f_2}{2}\right)$
A - B
Note that both envelope and carrier are in quadrature with A + B
(b)
A + B rectified
= |A + B|
A - B rectified
and inverted
= -|A - B|
+
(c)
|A + B| - |A - B|
frequency = $f_1 + f_2$
(d)
after band-pass
filtering
residual a.m. is removed by limiting

Fig. 7.1. — Interpolation between f.m. signals

before, because mixing is more reliably carried out at lower frequencies where stray reactive effects are less important. Binary dividers also have a limiting action which is very useful in view of the theoretical requirement that the two input signals should be of equal amplitude.

7.2. Chrominance a.g.c. unit

As mentioned in Section 6, the purpose of the chrominance a.g.c. unit is to correct variations in the amplitude of the 4·5 MHz colour subcarrier caused by changes in response of the different signal paths through the converter. Subjective tests[17] have shown that systematic fluctuations in subcarrier amplitude should not exceed 0·1 dB.

In the a.g.c. unit, the signal variations are corrected by passing the chrominance signal through a gain-controlled amplifier which is adjusted (during the colour-burst period) according to a comparison of the burst level with a reference level. Because each colour-burst always travels by the same path as the succeeding television line, it follows that if the amplifier gain is held at this value for a period of one line, then the chrominance signal will also be of the correct level. By repeating the level-comparison and gain-readjustment process for each combination of colour-burst and following line, the total chrominance signal is maintained at a substantially constant level.

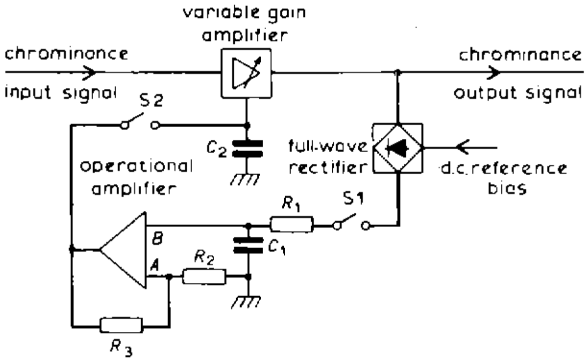

Fig. 7.2. – Chrominance a.g.c. schematic

Fig. 7.2 is a block diagram of the chrominance a.g.c. unit; the method of operation is as follows.

A d.c. signal proportional to the amplitude of the colour-burst is obtained by applying the chrominance output signal to a full-wave rectifier, the output of which is then sampled during the burst period by means of switch S1. The resultant signal is then used to control a variable-gain amplifier via integrating network $R1/C1$, an inverting amplifier and the sample-and-hold circuit comprising S2 and $C2$. The gain-control element is a field-effect transistor acting as a variable resistance the value of which depends on a control signal applied to the transistor gate. S2 opens just before the end of each burst; $C2$ charges to the sampled potential, and this 'stores' the control signal so obtained for the duration of the following line (i.e. until the next burst).

The integrating network $R1, C1$ controls the time constant of the feedback loop, and the value chosen for this (about 1 μs) is a compromise between two opposing factors. The speed of operation of the feedback loop should be such that any error in burst amplitude is substantially corrected within the burst period; conversely, it must be sufficiently slow to reject spurious error-signals resulting from noise or other interference pulses present during the sampling period. The choice of time-constant was dictated by these considerations. Note that the burst duration is about 4·6 μs, which is twice that normally used.

Theoretically, the control accuracy of an a.g.c. system such as that described varied in proportion to the gain round the feedback loop. Unfortunately, certain side effects caused by unwanted burst-gate switching pulses become increasingly troublesome with increase of loop gain, which must therefore be restricted. The permissible gain is, however, sufficient to reduce the burst-level variations found in practice to an imperceptible amount.

The (maintained) level of the chrominance signal at the output of the a.g.c. unit is controlled by providing adjustment of the d.c. reference voltage.

7.3. Fast-acting phase-error correction

7.3.1. Introduction

For the reasons discussed in Section 6 of this report, direct timing-correction of the intermediate signal output from the main store of the converter was not considered to be practicable. Instead, the intermediate signal is first partly decoded into a luminance and two colour-difference signals and timing correction is then carried out separately on each of these three components. A difficulty with this method, however, is that the 4·5 MHz decoding reference-subcarrier must be adjusted in phase at the beginning of each television line. This process[18] is performed in a unit called the 'fast phase-error corrector'; its position in the output signal-processing path can be seen in Fig. 6.7.

Subjective tests[17] showed that an accuracy of ±0·6° was required from the phase-error corrector; the performance achieved in the practical unit is ±1·2° and has proved to be satisfactory.

7.3.2. Principle of operation

Fig. 7.3 is a block diagram showing the principle parts of the fast phase-error corrector. The colour burst, of arbitrary phase, is gated out from the input video signal and, after amplitude limiting, is fed to two phase-detectors. Each phase-detector is also fed with a 4·5 MHz reference signal, the phase of one feed being disposed at 90° to the other. Thus, the outputs of the phase-detectors during the burst period comprise pulses with amplitudes and polarities proportional to the components of the burst signal resolved along quadrature axes shown as 'X' and 'Y' in Fig. 7.4(*a*).

The pulse outputs of the phase-detectors are applied to sample-and-hold circuits and then used to modulate quadrature feeds of 4·5 MHz reference subcarrier. This

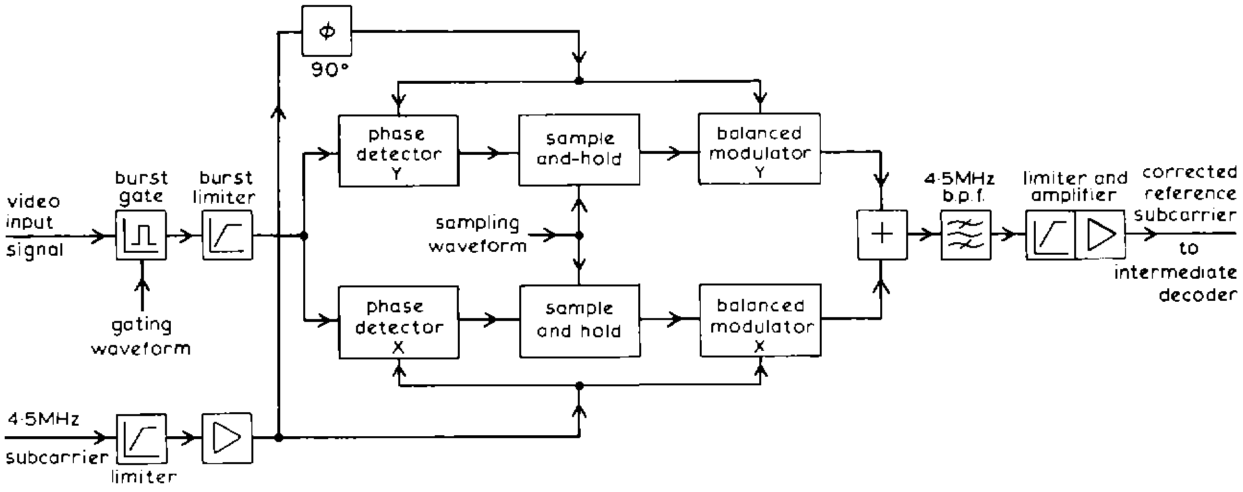

Fig. 7.3. — Fast phase-error corrector

process is carried out by balanced modulators which are identical in circuit to the phase-detectors previously described (and with which they are paired). As shown in Fig. 7.3, each 'pair' (comprising a phase-detector and a balanced modulator) employs one of the quadrature feeds of reference subcarrier.

The subcarrier output from each modulator is therefore identical in phase (ideally) to the burst component resolved by the associated phase detector; when the modulator outputs are added together (vectorial addition), the resultant is a reference subcarrier having a phase which is constant for one television line, and which is equal to that of the originating burst. This is shown in Fig. 7.4(*b*).

The output from the adder is filtered to remove components outside the chrominance band and, after amplifying and limiting, is fed to the intermediate-signal decoder.

7.4. R.F. group delay and amplitude equalisation

The converter is formed from a switched network of ultrasonic quartz delays and the group delay and amplitude responses of each unit should be equalised to within ±4 ns and ±0·2 dB, respectively, over a bandwidth of 10 MHz from 25 MHz to 35 MHz. This specification is necessary in order to prevent the cumulative error becoming large enough to produce visible patterns[2] on the output picture when groups of delay lines are switched in and out during the conversion process.

Response limitations arise from the characteristics of the fused quartz delay line itself,[19,18] those of the transducers[19,18] and those of their external circuits, in order of increasing accessibility of adjustment. Taking these in turn, the loss and delay in the quartz are both functions of the temperature and require a very stable high-temperature environment; in addition, the thickness of the quartz plate determines the uniformity of the delay and imperfections in the material may introduce undesirable ripples in the responses. The transducers and their mechanical tuning and damping account for most of the loss in the delay line and determine the limits of the passband. The specification[8] of a delay line and its transducers usually includes broad limits to the response variations within a stated passband, recognising that it would be impracticable to achieve the ultimately-desired uniformity without individual equalisation in the external amplifiers. The purpose of these amplifiers is to raise the signal to a high level at the input transducer, to retrieve it from a low level at the output transducer and to equalise the response to give a uniform-delay, unity-gain unit.

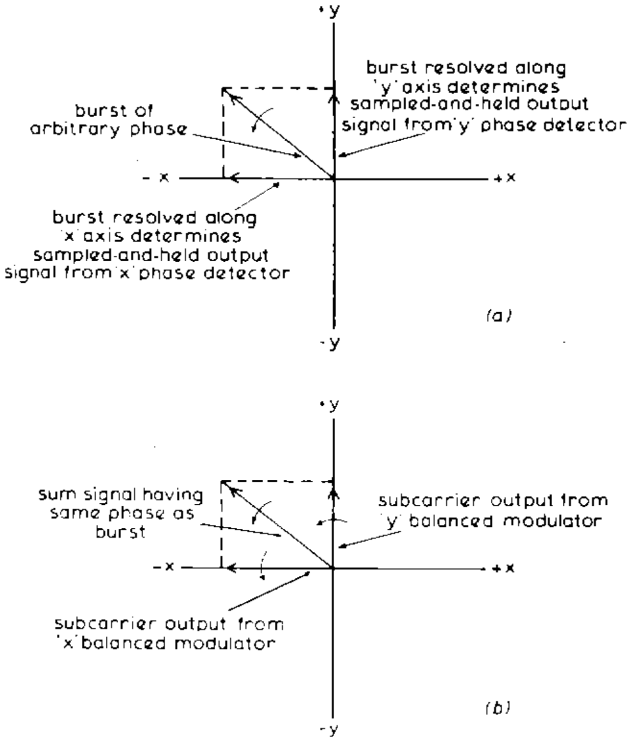
+y
burst of arbitrary phase
burst resolved along 'y' axis determines sampled-and-held output signal from 'y' phase detector
-x
+x
burst resolved along 'x' axis determines sampled-and-held output signal from 'x' phase detector
(a)
-y
+y
sum signal having same phase as burst
subcarrier output from 'y' balanced modulator
-x
+x
subcarrier output from 'x' balanced modulator
(b)
-y

Fig. 7.4. — Fast phase-error corrector: principle of operation

At the input transducer, the problem is to maintain a high signal-voltage level across the capacitance of the transducer without bandwidth restriction, group-delay distortion or non-linearity.

The circuit configuration and the use of a quarter-wave transformer enable the last stage of the amplifier to be removed from the high-temperature environment and to operate into a more nearly resistive load. In addition the circuit may be adjusted to give a first-order compensation for the response of the delay line.

At the output transducer, it is relatively easy to design a solid-state high-gain pre-amplifier to operate close to the output transducer and to effect a suitable compromise between the bandwidth and the signal-to-noise ratio.

The overall equalisation of the delay unit is achieved, after the output pre-amplifier, at a level of about 150 mV, at which it is convenient to measure the responses to be equalised and assess the number and type of equalisers.

A philosophy of equalisation indicates two different practical approaches to the same solution. One might, for example, first measure the response to be equalised and then, with the aid of a computer, construct individual equalisers giving the best theoretical result using a limited number of classical, passive, all-pass, group-delay equalisers and constant-resistance amplitude equalisers, leaving nothing to chance or subsequent adjustment. This approach might be easily automated for quantity production but is tiresome during development. Alternatively having first constructed equipment to give a simultaneous and continuous display of the responses of the delay unit over the desired bandwidth, new forms of equaliser could be developed having independent adjustments of sufficient range to cope with all likely requirements and finally achieve the desired result by inspection.

This 'adjust on test' approach demands considerable expertise; nevertheless, it was chosen for the following reasons. First, the problem of producing about hundred individual equalisers is less formidable when there are only a few basic types and, second, a design of active equaliser had already been developed[20,21,22] which was superior to the classical, passive equivalent both in flexibility and in tolerance of component values.

Active all-pass networks were described in 1964 by Kiefer of IRT in connection with equalisation of vestigial-sideband filters and this led to some unpublished work in 1965 by J.B. Izatt of BBC Research Department. The types of equaliser used in the Field Store Standards Converter[22] may be regarded as extensions and simplifications of Izatt's networks.

Simplified circuit diagrams, vector diagrams and responses for the group delay and amplitude equalisers are shown in Fig. 7.5 and Fig. 7.6 respectively. Both types of equaliser depend for their operation on the properties of a single tuned LC circuit and they have four adjustments which control centre frequency, bandwidth, amplitude and symmetry. They are designed to be cascaded so that the input impedance of one equaliser provides the preceding equaliser with the low-impedance load necessary for current addition and isolation.

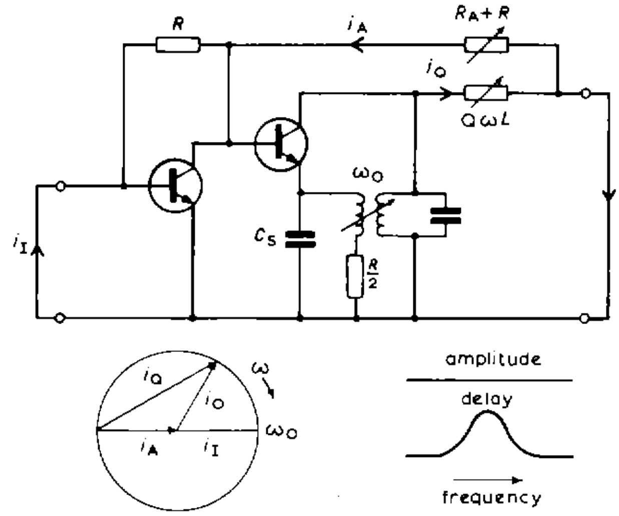

Fig. 7.5. – Basic group delay equaliser

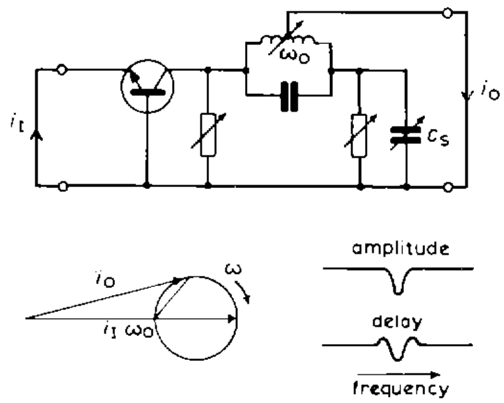

Fig. 7.6. – Basic amplitude equaliser

In the group-delay equaliser, Fig. 7.5, the current rejected by the tuned circuit is combined with part of the input current to give the output current a circular vector-locus centred on the origin. This results in an all-pass characteristic with a peak group delay at the resonant frequency and in ease of control of the bandwidth and centre frequency. Also the origin of the vector-locus may be shifted from the centre of the circles to allow the amplitude to rise or fall at the centre frequency and to adjust the symmetry of the response.

In the amplitude equaliser, the tuned circuit is balanced about its centre so that the vector vanishes and the output and input current are the same. By upsetting this balance slightly, a minimal-phase-shift contribution is made to the output current so as to produce a rise or fall at the centre frequency.

The number of these equalisers required for a delay unit has been found to be between one and four; if the conventional, passive circuits had been used, the number would be approximately doubled.

7.5. Signal parameters

The more important signal parameters, spectra and waveforms are detailed in Table 1 and illustrated in Fig. 7.7, respectively.

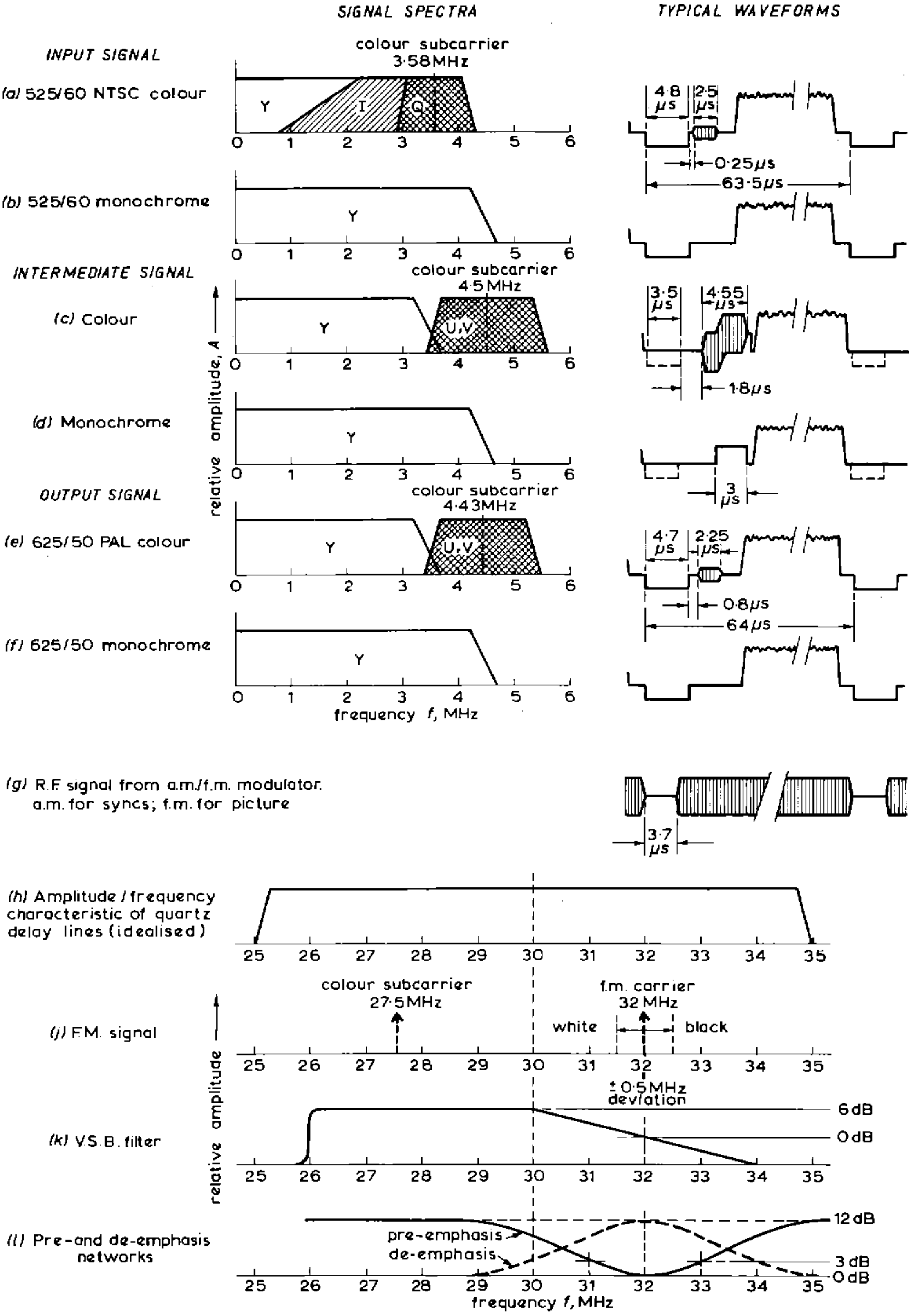

Fig. 7.7. – Spectra and waveforms

TABLE 1

Signal Parameters

Item	Unit	525/60 Input Signal	Intermediate Signal	Converted 625/50 PAL Output Signal
Field frequency	Hz	colour 59·9400 mono. 60·0000	–	50·0000 50·0000
Field period	ms	colour 16·683 mono. 16·667	–	20·000 20·000
Converter acceptable input field frequency range	Hz	colour 59·940 ± 0·004 mono. 60·000 ± 0·016	–	–
Line frequency (f_L)	Hz	colour 15,734·264 mono. 15,750	–	15,625 15,625
Line period	μs	colour 63·556 mono. 63·49	–	64·00 64·00
Colour subcarrier frequency (f_{sc})	Hz	3579545 ± 10	4500000 ± 13	4433618·75 ± 1
Relationship between f_{sc} and f_L		$f_{sc} = (227 + ½)f_L$	$f_{sc} = 286 f_L$*	$f_{sc} = (284 - ¼)f_L + 25$
Line blanking period	μs	colour 10·5 to 11·4 mono. 10·2 to 11·4	10·7 ± 0·1	12·05 ± 0·25
Line sync pulse width	μs	colour 4·2 to 5·1 mono. 4·2 to 5·7	3·5 ± 0·1	4·7 ± 0·1
Field blanking period		19 to 21 lines and line blanking	–	25 lines and line blanking
Burst duration	Cycles**	8^{+2}_{-0}	21 ± 1	10 ± 1
Luminance bandwidth	MHz	colour 4·2 mono. 4·2	3·25 4·2	3·25 4·2
Coded colour bandwidth	MHz	I, +0·6 to −1·8 Q, ± 0·6	U, ± 0·8 V, ± 0·8	U, ± 0·8 V, ± 0·8

* i.e. *input* line frequency

** i.e. cycles of colour subcarrier

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